Chapter 1

Features of Foundation Series 1.5

Welcome to Xilinx's newest software release, known as Foundation® Series 1.5. Xilinx is the world's largest supplier of programmable logic solutions, including industry-leading device architectures and world-class design software.

This release contains many enhancements and additions. The result is a product that provides hardware designers with an improved suite of tools for designing and implementing Programmable Logic Devices (PLDs).

If you ordered the Base Express or Foundation Express product, then you also received the Synopsys® HDL synthesis and optimization tool that can be used to create designs from VHDL and Verilog® HDL. See the **"In-Depth Tutorial — HDL-Based Design" chapter** in this manual for a detailed discussion on designing with HDL. Also see the **"HDL Design Entry and Synthesis" chapter** in the *Foundation Series User Guide* for information on how to use the Foundation GUIs to analyze, optimize, and synthesize HDL designs.

Refer to the Foundation Express online DynaText documentation, *VHDL Reference Guide* and *Verilog Reference Guide,* for information on how to use VHDL and Verilog to create designs.

This chapter contains the following sections:

- **"Xilinx Device Support"**
- **"New Features"**
- **"Tools and Applications"**

Note: Foundation Series 1.5 is intended for use with the Xilinx design implementation tools, such as PAR, MAP, and FIT. Compatibility with the XNF (logical) design files that were used in previous XACT*step* releases has been preserved.

To see a step-by-step installation procedure, see the "Installing Foundation" chapter in the *Foundation Series 1.5 Install and Release Document*.

Xilinx Device Support

Foundation Series 1.5 supports all available devices in the following families.

- XC3000A/L
- XC3100A/L
- XC4000E/L/EX/XL/XV/XLA
- XC5200
- Spartan/XL
- Virtex
- XC9500/XL

For further details about device support, refer to the "Device and Package Support" chapter in the *Foundation Series 1.5 Install and Release Document* that you received with this software.

Note: Technical information for all but the latest families is included in the Xilinx *Programmable Logic Data Book*. For the most up-to-date information about new devices, see the Xilinx Web Site at http://www.xilinx.com.

New Features

These are the major new features supported for this release.

- New FPGA and CPLD families in the release (XC4000XLA, XC9500XL, SpartanXL, and Virtex)
- Fully integrated design environment with automated design processing
  The Foundation Series Project Manager is the first design environment which integrates the Xilinx implementation tools. Furthermore, the HDL project management capabilities provided as part of Synopsys' FPGA Express are seamlessly integrated into the Foundation Series "Unified Project Manager." This embedding of the industry's most powerful FPGA design tools provides dramatic improvements in the project management revision control capabilities. The new Foundation Series design flows also feature powerful, push-button compilation without sacrificing design performance or runtime.
- New synthesis technology
  The Foundation Series Base Express and Foundation Express product configurations both feature HDL synthesis from Synopsys FPGA Express. This release of the Foundation Series enables true HDL design flows as well as mixed-language (VHDL and Verilog HDL) synthesis and optimization. Support for mixed-language design flows is becoming increasingly important as the use of third party or inter-organizational Intellectual Property (IP or cores) grows. Check out the **"Foundation Express" section** in this chapter to learn more details about the Foundation's synthesis capabilities.
- New Xilinx Constraints Editor enabling easy system performance specification. The Editor is accessible from the Start button (**`Start` → `Programs` → `Xilinx Foundation Series` → `Accessories` → `Constraints Editor`**).
- JTAG Programmer now supports both CPLDs and FPGAs for download and configuration. Supported families include XC4000E/L/EX/XL/XV/XLA, XC5200, XC9500/XL, and Spartan/XL.
- Redefined 1.5 Project Flows: Schematic and HDL
  An HDL Flow contains VHDL and Verilog top-level designs with optional black boxes and HDL modules. The entire design is always exported in HDL terms and synthesized.
  Any black boxes in the design are passed to the implementation tools for translation. For details, see the **"Design Methodologies - HDL Flow" chapter** in the *Foundation Series User Guide*.
  A Schematic Flow may only have schematic designs as top-level designs. These top-level designs can contain HDL modules, Finite State Machine macros, and LogiBLOX modules. For details, refer to the **"Design Methodologies - Schematic Flow" chapter** in the *Foundation Series User Guide*.
- Updated CORE Generator™ System
  The Xilinx CORE Generator is an easy-to-use design tool that delivers parameterizable cores, optimized for Xilinx FPGAs. This library includes cores as complex as DSP filters and multipliers, and as simple as delay elements. You can use these cores as building blocks in order to complete your designs more quickly. The cores have been completely tested for compatibility with Foundation 1.5 Software.
  The Xilinx CORE Generator CD-ROM is included with your Foundation 1.5 Series Software contents. You will find the CD-ROM in its own case, along with installation instructions on the case cover.

- New sample designs

  bcd_acc—A Verilog-based HDL Flow, this project is a design of a 4-digit BCD accumulator.

  calc3ka—This Schematic Flow implements a simple calculator in an XC3020A.

  flash—This Schematic Flow contains VHDL and LogiBLOX sub-modules. A free-running counter circuit is targeted to an XC4003 that you can download to the Xilinx demonstration board.

  gate—This HDL Flow implements a movement/direction detector in Verilog.

  hex2bin—This Schematic Flow contains Verilog, LogiBLOX, and CORE Generator sub-modules. It converts Intel hex-formatted data to binary format and stores it into an external 64Kb memory array.

  JCT—This collection of designs supports the CPLD-specific JCOUNT tutorial, found in the on-line Foundation Help system.

  A Johnson counter is implemented using several design methods: VHDL, ABEL, schematic, schematic with an embedded VHDL macro, and schematic with an embedded ABEL macro.

  uart—A top-level ABEL project of a UART receiver that is implemented with XABEL-CPLD synthesis tools.

  vtimer4e—An HDL Flow, this project contains a VHDL description of a programmable timer.

  watch—This collection of designs is provided for use with the main Foundation tutorial, which can be found in this manual, the Quick Start Guide. A stopwatch is implemented in the two Project Flows: Schematic and HDL. (Both VHDL and Verilog versions are provided for the HDL Flow.)

- HDL Simulation Capabilities

  Foundation Series Software v1.5 now provides the option of adding HDL simulation capabilities to all Foundation design flows. The demand for HDL simulation capabilities has grown as Xilinx provides higher density silicon solutions. To meet this need, Xilinx is shipping an evaluation version of HDL simulators from both Aldec, Incorporated and MTI with this release.

  Both of these products may be licensed for evaluation free for up to 30 days. Sale and support for both of these products is provided directly by the vendors.

  Active-VHDL product sales are handled directly by Aldec, Inc. and its authorized distributors (email sales@aldec.com).

  Customer support is also provided directly by Aldec, Inc. (emailsupport@aldec.com)

  You can access the Active-VHDL simulator from the Project Manager (**`Tools`** → **`Simulation/Verification`** → **`ACTIVE-VHDL Behavioral Simulation`**).

  The addition of Active-VHDL to your Foundation Series design environment provides a complete VHDL development environment. This complete development environment includes source code debugging, functional and back-annotated timing simulations, as well as a comprehensive verification methodology based on the use of VHDL testbenches.

  All ModelSim product sales are handled directly by MTI and its authorized sales affiliates (email sales@model.com).

  Customer support is also provided directly by MTI (email support@model.com or call the main number at (503) 641-1340)

  Adding MTI's ModelSim product to the Foundation Series design environment enables simulation of VHDL, Verilog HDL or mixed-HDL designs (Verilog and VHDL). Source code debugging, functional simulation and back-annotated timing simulation are all supported through this integrated solution. The availability of a mixed-language simulation environment offers maximum flexibility to HDL design methodologies which draw on design elements from both Verilog and VHDL.

- CPLD enhancements

Enhancements in logic optimization and fitting technology have generated faster system clock frequencies, for push-button and timing driven implementations, as well as faster compilation runtimes, averaging 36% improvement.
The XC9500/XL devices are now fully supported in the LogiBLOX module synthesis technology, allowing increased logic utilization for both schematic and HDL-based designs.

Tools and Applications

This section describes specific tool and application program behavior changes for this release.

Foundation Project Manager

The Foundation Project Manager—the overall project management tool—contains the Foundation Series tools used in the design process. Within the Project Manager, you access the design entry tools, functional simulation, the design implementation tools, timing simulation, and design verification. Major new Project Manager features include the following.

- New Graphical User Interface (GUI)
  The new Project Manager GUI includes new tabbed windows for the Hierarchy Browser and for the Message Console window that displays the project log and HDL related tabs (HDL Errors, HDL Warnings and HDL Messages) for HDL projects.
  The Project Manager GUI has a new flow chart layout and redesigned menus. The most common commands are available from shortcut menus.

- New Hierarchy Browser
  The Hierarchy Browser now displays two tabs, Files and Versions. The Files tab shows the design documents hierarchy using redesigned icons. The Versions tab shows the status of design chip implementation.
  The new Versions tab shows common design management features: design operations available from context-sensitive shortcut menus and implementations and version/revision management.

- New Project Flowchart
  The new Project Flowchart provides direct access to synthesis and implementation tools from the Project Manager window. For implementation, you can run Translate, Map, Place and Route, Fit, Configure, Bitstream, JTAG Programmer, Hardware Debugger, and PROM File Formatter by clicking the appropriate flowchart phase buttons.

- Context-Sensitive menus
  Commands for all design processing are available from context-sensitive shortcut menus. The shortcut menus are invoked by clicking the items selected on the Versions tab with the right mouse button.

- Full integration of synthesis processing
  Synthesis of VHDL and Verilog using the FPGA Express synthesis technology is now fully integrated within the Project Manager. Seamless HDL synthesis is supported for both all-HDL flows and mixed-level Verilog, VHDL designs.
  Timing and layout constraint creation is available using the Foundation Express Constraints Editor if you have a license for the "Foundation Express" configuration. In the Versions tab, right click on the functional structure of a project version and then select Edit Constraints to open the Express Constraints editor. Use the Xilinx Constraints Editor for entering constraints if you have other licensed Foundation configurations.
  The Express Constraints Editor is available from the Versions tab of the Hierarchy Browser. Right click on the Version to access the pulldown menu for Edit Synthesis Constraints.

- Design conversions
  Previous M1 Foundation designs can be converted to 1.5. After opening the old design in the Project manager, select **File → Project Type**. Note that this is a one way conversion, that is, you cannot convert designs from 1.5 to 1.4.
  If your old design contains any VHDL modules, see the *Metamor to Express Conversion Guide* application note. You can access this application note from the Foundation Help by selecting **Help → Foundation Help Contents** and then selecting **Application Notes**.

Logic Simulator

- New simulation script wizard
  The new wizard simplifies the process of creating simulation automation scripts.
- Improved performance. The new version of the simulator runs significantly faster than the previous version.
- Signal Selection dialog box improvements
  The following changes have been applied to the Component Selection for Waveform Viewer dialog.
  - The Search option operates on all items, not only on those currently loaded in the list box.
  - Signals and chips are not automatically sorted before the dialog box is opened. Instead of the automatic sorting, the Sort button is added to the Signal Selection pane of the Component Selection dialog. The signals in the list box can be sorted by clicking the Sort button.
- Preferences enhancements (**Options → Preferences**)
  An additional check box, Enable Global Netlist Analysis, has been added to the General tab of the Preferences dialog box.
  Unchecking this option may speed up the process of loading netlists. Global Netlist Analysis is the final phase of netlist loading that checks interblock connections. It is not necessary to perform this analysis each time the netlist is loaded. You may execute it only once to check whether all connections are correct and then switch this option off. This setting has to be set for each project separately.

Schematic Editor

Following is a list of enhancements to the Schematic Editor.

- New bus model and behavior
  - Buses now behave more like wires when edited and moved.
  - The bus model has been revised. Complex buses, in the form of the list of single signals and simple buses, separated by commas, is now implemented. Complex buses use the bus label format that follows.
    NAME[*l*:*h*], *NAME*, *NAME*[*l*:*h*]
    NAME is the bus label or the net label.
    l is the first number.
    h is the last number.
    Following is an example.

C[0:3], B, A[2:4]

  - Conversion of the older bus format is provided to enable loading schematics created with older software versions.
  - Descriptions of bus connections are changed into bus labels during loading.
  - Buses that cross each other in a schematic are now interpreted as separate buses, that is, non-connected.
  - Symbol pins in the form of complex buses are implemented for Create Macro Symbol from Current Sheet.
  - Editing complex bus pins in the Symbol Editor is now available.
  - Simple buses format xxxx[r1:r2]yyyy are supported.

- Context-sensitive menus
  The commonly used commands are now accessible from local, context-sensitive shortcut menus. Shortcut menus appear when certain items are clicked with the right mouse button. Their contents depend on the current context.
- Selecting wires
  The Select All command or selecting a rectangle part of a schematic using the mouse, now selects all wires instead of selecting only components.
- Smart deletion of wires
  When symbols representing blocks are deleted, only those wires that are internal to the selected block are deleted.
- Nets and buses enhancements
  - Improved autowire behavior; rubberbanding
  - Editing buses similar to editing wires
- Improved Symbol Selection dialog box
  Symbols in the Symbol Selection dialog box are now grouped by library which are displayed in bold. Symbols belonging to the library are listed by double clicking the library name. The listing can be closed by double clicking the library name once more.
- Improved Replace Symbol dialog box
  The Replace Symbol dialog box now has an additional option to replace symbols in the selected area on the current schematic sheet, apart from replacing all symbols on the current sheet. Additionally, the With Symbol: Box is now a drop-down list of available symbols, from which you can select the desired one.
- Dragging of attributes, references, and symbol names
  Dragging of attributes, references, and symbol names is now available after selecting them on schematics. You do not have to open the Symbol Properties dialog box to select the Move option for the items these items.
- Multilevel Undo command
  The Undo command now allows for multiple-level reverse editing (five levels are now available).

- Improved Copy/Paste option
  Pasting of a selected schematic area displays the schematic area contents (symbols, nets). When pasting a copied region onto a schematic, the copy's contents display as it is moved which makes it easy to line up pins between the copy and the schematic.

Finite State Machine (FSM) Editor

- Verilog code generation support
  In addition to VHDL and ABEL code generation from state diagrams, there is now an option to generate Verilog code.
- Template optimization
  The FSM editor generates VHDL or Verilog code based on templates that are optimized for the Express Synthesis engine.
- Foundation Express synthesis
  Foundation Express, powered by Synopsys FPGA Express Synthesis technology, is now available for both Verilog and VHDL synthesis.

HDL Editor

- Verilog support
  - Color coding of Verilog source files
  - Specific language and synthesis templates available for Verilog
  - Syntax checking and synthesis of Verilog source files by the Foundation Express tool.
- Foundation Express synthesis and check syntax
  Within the HDL Editor, the Foundation Express tool performs syntax checking and synthesis (for schematic only)
- New VHDL and Verilog language and synthesis templates
  New templates specific for Foundation Express are now available for VHDL and Verilog source files.
- New Insert File option
  The new Insert File option is now available from the Edit menu. With this option, you can insert the contents of a file into an HDL Editor document making component instantiation easier (for example, LogiBLOX).

Foundation Express

The Synopsys FPGA Express synthesis engine has been integrated within the Foundation Project Manager, Schematic Editor, HDL Editor, and State Diagram Editor.

This new synthesis engine provides the following:

- Support for all new devices including SpartanXL/XV, Virtex, XLA, and XC9500XL
- Initial support added for VHDL IEEE Std 1076-1993
  `end entity` *entity_name*;

end architecture *architecture_name*;
end component *component_simple_name*;
end configuration *configuration_name*;
end package *package_name*;
end package body *package_body_name*;
end record *record_simple_name*;
component *component_name* **is**
[*label***:**] **process** [**(***sensitivity-list***)**] **is**
*label***: component** *component_name*
*label***: s0 <= a and b;**
'IMAGE(*X***);**
block declarations in a generate statement
(VHDL LRM section 9.7)
alias keyword (type must be declared)

- Expanded VHDL language support
  rising_edge(CLK)
  falling_edge(CLK)
  bus(5 downto 2) <= (others => '0');
  (array slices with others)
- Post-synthesis HDL simulation netlists
  VHDL and Verilog functional netlist are now available after synthesis optimization.
- VHDL state machines
  VHDL designs containing one-hot encoded state machines are typically improved by 15 to 20% in both speed and area.

Design Implementation Tools

Following is a list of new features in the design implementation tools.

New Features

- Security licensing eliminated for Base and Standard
  The FLEXlm Software security licensing for both Base and Standard users has been replaced by a numbered CD key. The key is used for software installation; a sticker with your key number is located on the back of your Design Entry/Implementation Tools CD-ROM. You no longer need to call Xilinx to obtain registration numbers for installation of Base and Standard packages. Furthermore, you no longer need to set up the LM_LICENSE_FILE environment variables. However, you must still obtain a permanent license for Base Express and Foundation Express.
- Support for SpartanXL/XV, Virtex, XLA, and XC9500XL
- Runtime improvements
  Runtime throughout the system has been improved dramatically. The biggest decrease will be seen in the timing-driven place and route times, but there are also six to ten times faster runtimes in the design translation and back-annotation programs. In addition, there are new timing analysis algorithms that easily handle the growing number of timing paths associated with larger designs.
  See the **"PAR—Place and Route" chapter** and the **"TRACE" chapter** in the online DynaText document,

Development System Reference Guide for details.

- Constraints Editor GUI
  For Foundation series customers who are not licensed for Express, Xilinx has created a Constraints Editor that simplifies the creation of timing and layout constraints.
  Now you can enter timing and physical constraints using a graphical user interface. Timing constraints and I/O pin locations can quickly and easily be specified for any design. Detailed controls are also available without the need to know the constraint language syntax.

- Floorplanner
  The Xilinx Floorplanner is a graphic tool you can use interactively. It automatically places logic from a hierarchical design into a Xilinx FPGA. Both detailed placement and area-based floorplanning can be accomplished using this program.
  The tool is now available for the Spartan/XL and XC4000E/EX/XL/XLA/XV families. For a complete description of this tool, see the online DynaText document, *Floorplanner Reference/User Guide*.

Program Behavior Changes For 1.5

The following section describes program behavior changes for this release.

- Automatic pin-locking
  I/O pins can now be locked to a previous revision by simply selecting the revision in the Versions tab of the Project Manger and selecting (**`Tools` → `Implementation` → `Lock Device Pins`**).

- Minimum path delay reports
  You can now get a minimum delay report from the Timing Analyzer program (trce) or the simulation back-annotation programs for the XC4000XL family. Support for other families will be provided through software updates, which are available on the Xilinx web site. The web site address is http://www.xilinx.com.

- Temperature and voltage prorating
  New temperature and voltage settings can now be used to specify the true operating environment of the FPGA. Circuit performance can be substantially improved in a controlled environment, compared to general worst-case commercial ranges.
  For Release 1.5, these two constraints are supported only for the XC4000XL. Refer to the **"Prorating Constraints" section** in the online DynaText document, *Development System Reference Guide* for details.

- New and improved timing constraints
  - TNM_NET (For FPGA designs only)
    This new constraint solves the problems associated with clock names changing when a design is re-synthesized. It can be placed on the clock pad itself. The clock pad's name will not change. See the **"Creating User-Defined Groups Using TNM_NET" section** in the online DynaText document, *Development System Reference Guide* for details.

  - OFFSET
    This constraint now has a global capability to specify the input setup time of all I/Os associated with a specific clock and a single restraint. This can also be used to specify all clock to output paths. OFFSET also now accepts timegroups for registers and pads, allowing for the creation of fewer total constraints. See the **"OFFSET Timing Specifications" section** in the *Development System Reference Guide* for details.

- PERIOD
  PERIOD constraints can now be qualified with timegroups. Clock Skew is now taken into account when running timing analysis and timing driven place and route. With design speeds exceeding 100 Mhz and devices continually getting larger, even skew less than 1 ns is becoming important to account for.

- PAR (Place and Route) report improvements
  PAR now produces a timing constraint summary report upon the completion of place and route. In addition, a detailed report will automatically be produced by the timing tools for any constraints that have not been met. The PAD report has been improved to include special purpose pins on the device, such as VCC, GND, and BSCAN.
- Multi-Pass Place and Route and Guide Files are not accessible through the Foundation Project Manager. Access these functions through the standalone Design Manager (**Start → Programs → Xilinx Foundation Series → Accessories → Design Manager**).

Documentation

Two new online DynaText documents, *VHDL Reference Guide* and *Verilog Reference Guide*, describe how to use the Verilog and VHDL languages to create designs. If you have installed these manuals, you can access them from the online help as well as from the DynaText collection. To access from the online help, select **Help → Foundation Help Contents**. Under Reference click **VHDL Reference Guide** or **Verilog Reference Guide**.

The *Foundation Quick Start Guide 1.5* contains completely new in-depth tutorials that illustrate how to create, simulate, implement, and verify schematic and HDL designs.

The new interactive Foundation Demo, located on the documentation CD, illustrates how to use the Schematic Editor, State Diagram Editor, and Logic Simulator. The demo also shows how to create and synthesize an HDL design as well as implement a design. To invoke the demo, select **Start → Programs → Xilinx Foundation Series → Multimedia Foundation Demo**. You can access the demo if the files have been installed from the documentation CD or if the documentation CD is installed in the caddy.

Online help contains new and updated information.

- The Basic FPGA Design Flow tutorial provides more information about HDL designs.
- The FPGA Design Techniques has more Verilog examples.
- A new section called Project Flows, located under Techniques in the umbrella help, describes the F1.5 schematic and HDL flows.
- Help for the Foundation implementation tools can be invoked directly from the umbrella help.
- Three CPLD documents have been eliminated and their information merged into other CPLD help files.