Libraries Guide

Preface

About This Manual

This manual describes Xilinx's Unified Libraries and the attributes/constraints that can be used with the components.

Before using this manual, you should be familiar with the operations that are common to all Xilinx software tools: how to bring up the system, select a tool for use, specify operations, and manage design data. These topics are covered in the *Quick Start Guide*.

You must consult *The Programmable Logic Data Book* for device-specific information on Xilinx device characteristics, including readback, boundary scan, configuration, length count, and debugging. *The Programmable Logic Data Book* is available in hard copy and on the Xilinx web site (http://www.xilinx.com). See http://www.xilinx.com/partinfo/databook.htm for the current version of this book.

For specific design issues or problems, use the Answers Search function on the Web (http://www.xilinx.com/support/searchtd.htm) to access the following.

- Answers Database: current listing of solution records for the Xilinx software tools
- Applications Notes: descriptions of device-specific design techniques and approaches
- Data Sheets: pages from *The Programmable Logic Data Book*
- XCELL Journal: quarterly journals for Xilinx programmable logic users
- Expert Journals: the latest news, design tips, and patch information on the Xilinx design environment

If you cannot access the Web, you can install and access the Answers book with the DynaText online browser in the same manner as the Xilinx book collection. The Answers book includes information in the Answers Database at the time of this release.

Manual Contents

Online Manual

If you are viewing this manual online, it is divided into twelve chapters.

- Chapter 1, **"Xilinx Unified Libraries"**
- Chapter 2, **"Selection Guide"**
- Chapter 3, **"Design Elements (ACC1 to BYPOSC)"**
- Chapter 4, **"Design Elements (CAPTURE_VIRTEX to DECODE64)"**
- Chapter 5, **"Design Elements (F5MAP to FTSRLE)"**

- Chapter 6, **"Design Elements (GCLK to KEEPER)"**
- Chapter 7, **"Design Elements (LD to NOR16)"**
- Chapter 8, **"Design Elements (OAND2 to OXOR2)"**
- Chapter 9, **"Design Elements (PULLDOWN to ROM32X1)"**
- Chapter 10, **"Design Elements (SOP3 to XORCY_L)"**
- Chapter 11, **"Design Elements (X74_42 to X74_521)"**
- Chapter 12, **"Attributes, Constraints, and Carry Logic"**

Chapter 1, "Xilinx Unified Libraries," discusses the unified libraries, applicable device architectures for each library, contents of the other chapters, general naming conventions, and performance issues.

Chapter 2, "Selection Guide," describes then lists design elements by function that are explained in detail in the "Design Elements" chapters.

Chapters 3 through 11, "Design Elements," provide a graphic symbol, functional description, primitive versus macro table, truth table (when applicable), topology (when applicable), and schematics for macros of the design elements.

Chapter 12, "Attributes, Constraints, and Carry Logic," provides information on all attributes, logical constraints, placement and timing constraints, relationally placed macros (RPMs), and carry logic.

Conventions

Typographical

This manual uses the following conventions. An example illustrates each convention.

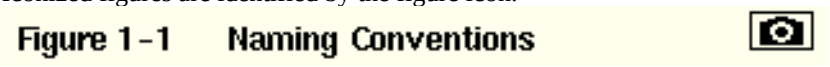
- `Courier font` indicates messages, prompts, and program files that the system displays.
  `speed grade: -100`
- **`Courier bold`** indicates literal commands that you enter in a syntactical statement.
  `rpt_del_net=`
  `Courier bold` also indicates commands that you select from a menu.
  `File → Open`
- *Italic font* denotes the following items.
  - Variables in a syntax statement for which you must supply values
    `edif2ngd` *design_name*
  - References to other manuals
    See the *Development System Reference Guide* for more information.
  - Emphasis in text
    If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.
- Square brackets "[ ]" indicate an optional entry or parameter. However, in bus specifications, such as bus [7:0], they are required.

`edif2ngd` [*option_name*] *design_name*

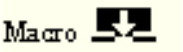
- Braces "{ }" enclose a list of items from which you choose one or more.
  `lowpwr = {on | off}`
- A vertical bar "|" separates items in a list of choices.
  `symbol` *editor_name* `[bus|pins]`
- A vertical ellipsis indicates repetitive material that has been omitted.
  ```
  IOB #1: Name = QOUT'
  IOB #2: Name = CLKIN'
  .
  .
  .
  ```
- A horizontal ellipsis ". . ." indicates that an item can be repeated one or more times.
  `allow block` *block_name loc1 loc2* `...` *locn;*

Online Document

Xilinx has created several conventions for use within the DynaText® online documents.

- Red-underlined text indicates an interbook link, which is a cross-reference to another book. Click on the red-underlined text to open the specified cross-reference.
- Blue-underlined text indicates an intrabook link, which is a cross-reference within a book. Click on the blue-underlined text to open the specified cross-reference.
- There are several types of icons.
  Iconized figures are identified by the figure icon.
  

  Iconized tables are identified by the table icon.
  

  The Copyright icon displays in the upper-left hand corner on the first page of every Xilinx online document.
  
  The DynaText footnote icon displays next to the footnoted text.
  

  Double-click on these icons to display figures, tables, copyright information, or footnotes in a separate window.
- Inline figures display within the text of a document. You can display these figures in a separate window by clicking on the figure.