Chapter 8

Design Elements (OAND2 to OXOR2)

This chapter describes design elements included in the Unified Libraries. The elements are organized in alphanumeric order with all numeric suffixes in ascending order.

Information on the specific architectures supported by each of the following libraries is contained under the Applicable Architectures section of the Unified Libraries Chapter.

- **XC3000 Library**
- **XC4000E Library**
- **XC4000X Library**
- **XC5200 Library**
- **XC9000 Library**
- **Spartan Library**
- **SpartanXL Library**
- **Virtex Library**

Note: Wherever *XC4000* is mentioned, the information applies to all architectures supported by the XC4000E and XC4000X libraries.

Note: Wherever *Spartans* or *Spartan series* is mentioned, the information applies to all architectures supported by the Spartan and SpartanXL libraries.

Schematics are included for each library if the implementation differs. Design elements with bused or multiple I/O pins (2-, 4-, 8-, 16-bit versions) typically include just one schematic — generally the 8-bit version. When only one schematic is included, implementation of the smaller and larger elements differs only in the number of sections. In cases where an 8-bit version is very large, an appropriate smaller element serves as the schematic example.

OAND2

2-Input AND Gate with Invertible Inputs

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
N/A	N/A	Primitive	N/A	N/A	N/A	Primitive	N/A

X6955

OAND2 is a 2-input AND gate that is implemented in the output multiplexer of the XC4000X IOB. The F pin is faster than I0. Input pins can be inverted even though there is no library component showing inverted inputs. The mapper will automatically bring any inverted input pins into the IOB.

OBUF, 4, 8, 16

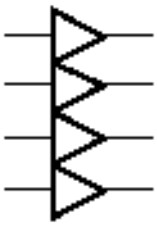
Single- and Multiple-Output Buffers

Element	XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	Spartan XL	Virtex
OBUF	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
OBUF4, OBUF8, OBUF16	Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro

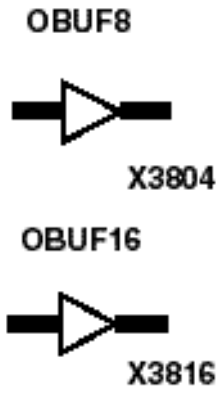
OBUF

X3785

OBUF4



X3792

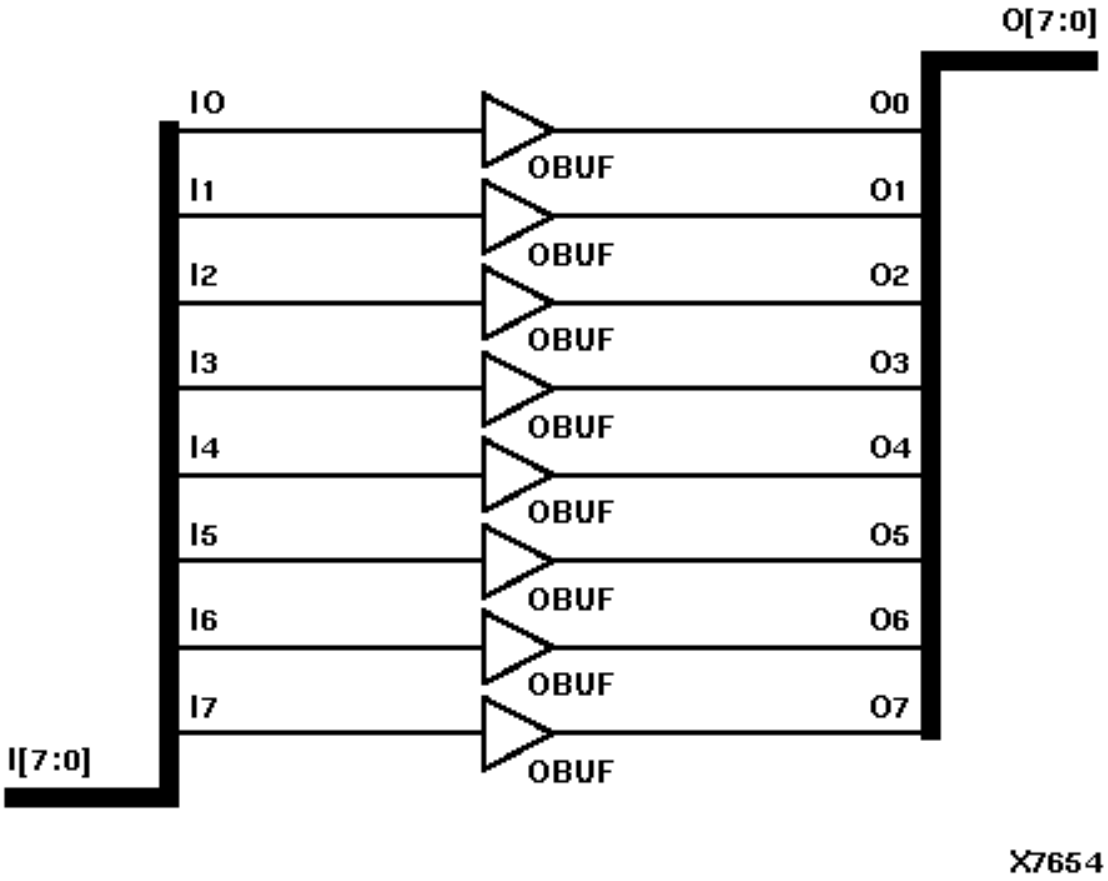


OBUF, OBUF4, OBUF8, and OBUF16 are single and multiple output buffers. An OBUF isolates the internal circuit and provides drive current for signals leaving a chip. OBUFs exist in input/output blocks (IOB). The output (O) of an OBUF is connected to an OPAD or an IOPAD.

For XC9000 CPLDs, if a high impedance (Z) signal from an on-chip 3-state buffer (like BUFE) is applied to the input of an OBUF, it is propagated to the CPLD device output pin.

For Virtex, refer to the **"OBUF_selectIO"** section for information on OBUF variants with selectable I/O interfaces. The I/O interface standard used by OBUF, 4, 8, and 16 is LVTTL. Also, Virtex OBUF, 4, 8, and 16 have selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

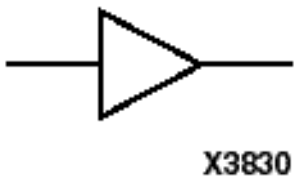
Figure 8-1OBUF8 Implementation XC3000, XC4000, XC5200, XC9000, Spartans, Virtex



OBUF_*selectIO*

Single Output Buffer with Selectable I/O Interface

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	N/A	N/A	N/A	N/A	N/A	Primitive



OBUF and its variants (listed below) are single output buffers whose I/O interface corresponds to a specific I/O

standard. The name extensions (LVCMOS2, PCI33_3, PCI33_5, etc.) specify the standard. The S, F, and 2, 4, 6, 8, 12, 16, 24 extensions specify the slew rate (SLOW or FAST) and the drive power (2, 4, 6, 8, 12, 16, 24 mA) for the LVTTL standard variants. For example, OBUF_F_12 is a single output buffer that uses the LVTTL I/O-signaling standard with a FAST slew and 12mA of drive power.

OBUF has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

An OBUF isolates the internal circuit and provides drive current for signals leaving a chip. OBUFs exist in input/output blocks (IOB). The output (O) of an OBUF is connected to an OPAD or an IOPAD.

The hardware implementation of the I/O standard requires that you follow a set of usage rules for the SelectI/O buffer components. Refer to the **"SelectI/O Usage Rules" section** under the IBUF_*selectIO* section for information on using these components.

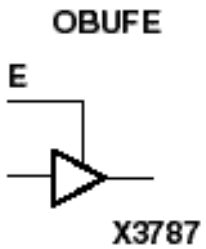
Component	I/O Standard	VCCO
OBUF	LVTTL	3.3
OBUF_S_2	LVTTL	3.3
OBUF_S_4	LVTTL	3.3
OBUF_S_6	LVTTL	3.3
OBUF_S_8	LVTTL	3.3
OBUF_S_12	LVTTL	3.3
OBUF_S_16	LVTTL	3.3
OBUF_S_24	LVTTL	3.3
OBUF_F_2	LVTTL	3.3
OBUF_F_4	LVTTL	3.3
OBUF_F_6	LVTTL	3.3
OBUF_F_8	LVTTL	3.3
OBUF_F_12	LVTTL	3.3
OBUF_F_16	LVTTL	3.3
OBUF_F_24	LVTTL	3.3
OBUF_LVCMOS2	LVCMOS2	2.5
OBUF_PCI33_3	PCI33_3	3.3
OBUF_PCI33_5	PCI33_5	3.3
OBUF_PCI66_3	PCI66_3	3.3
OBUF_GTL	GTL	N/A

OBUF_GTLP	GTL+	N/A
OBUF_HSTL_I	HSTL_I	1.5
OBUF_HSTL_III	HSTL_III	1.5
OBUF_HSTL_IV	HSTL_IV	1.5
OBUF_SSTL2_I	SSTL2_I	2.5
OBUF_SSTL2_II	SSTL2_II	2.5
OBUF_SSTL3_I	SSTL3_I	3.3
OBUF_SSTL3_II	SSTL3_II	3.3
OBUF_CTT	CTT	3.3
OBUF_AGP	AGP	3.3

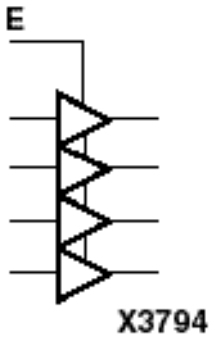
OBUFE, 4, 8, 16

3-State Output Buffers with Active-High Output Enable

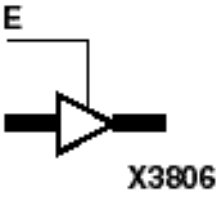
Element	XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	Spartan XL	Virtex
OBUFE	Macro	Macro	Macro	Macro	Primitive	Macro	Macro	Macro
OBUFE4, OBUFE8, OBUFE16	Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro



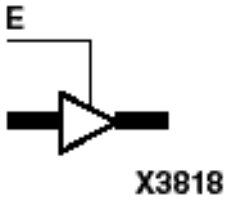
OBUFE4



OBUFE8



OBUFE16



OBUFE, OBUFE4, OBUFE8, and OBUFE16 are 3-state buffers with inputs I, I3 – I0, I7 – I0, and I15-I0, respectively; outputs O, O3 – O0, O7 – O0, and O15-O0, respectively; and active-High output enable (E). When E is High, data on the inputs of the buffers is transferred to the corresponding outputs. When E is Low, the output is High impedance (off or Z state). An OBUFE isolates the internal circuit and provides drive current for signals leaving a chip. An OBUFE output is connected to an OPAD or an IOPAD. An OBUFE input is connected to the internal circuit.

Inputs		Outputs
E	**I**	**O**
0	X	Z
1	1	1
1	0	0

Figure 8-2OBUFE Implementation XC3000, XC4000, XC5200, Spartans, Virtex

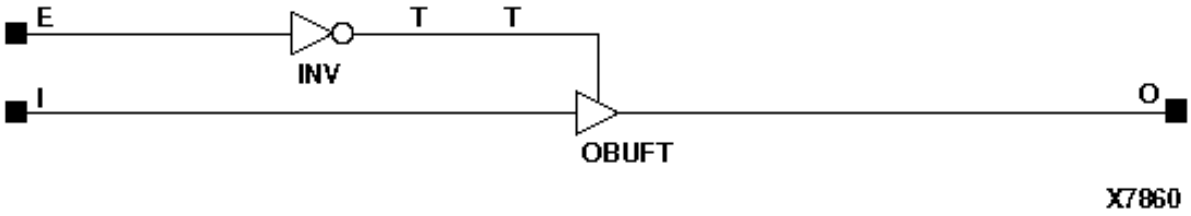
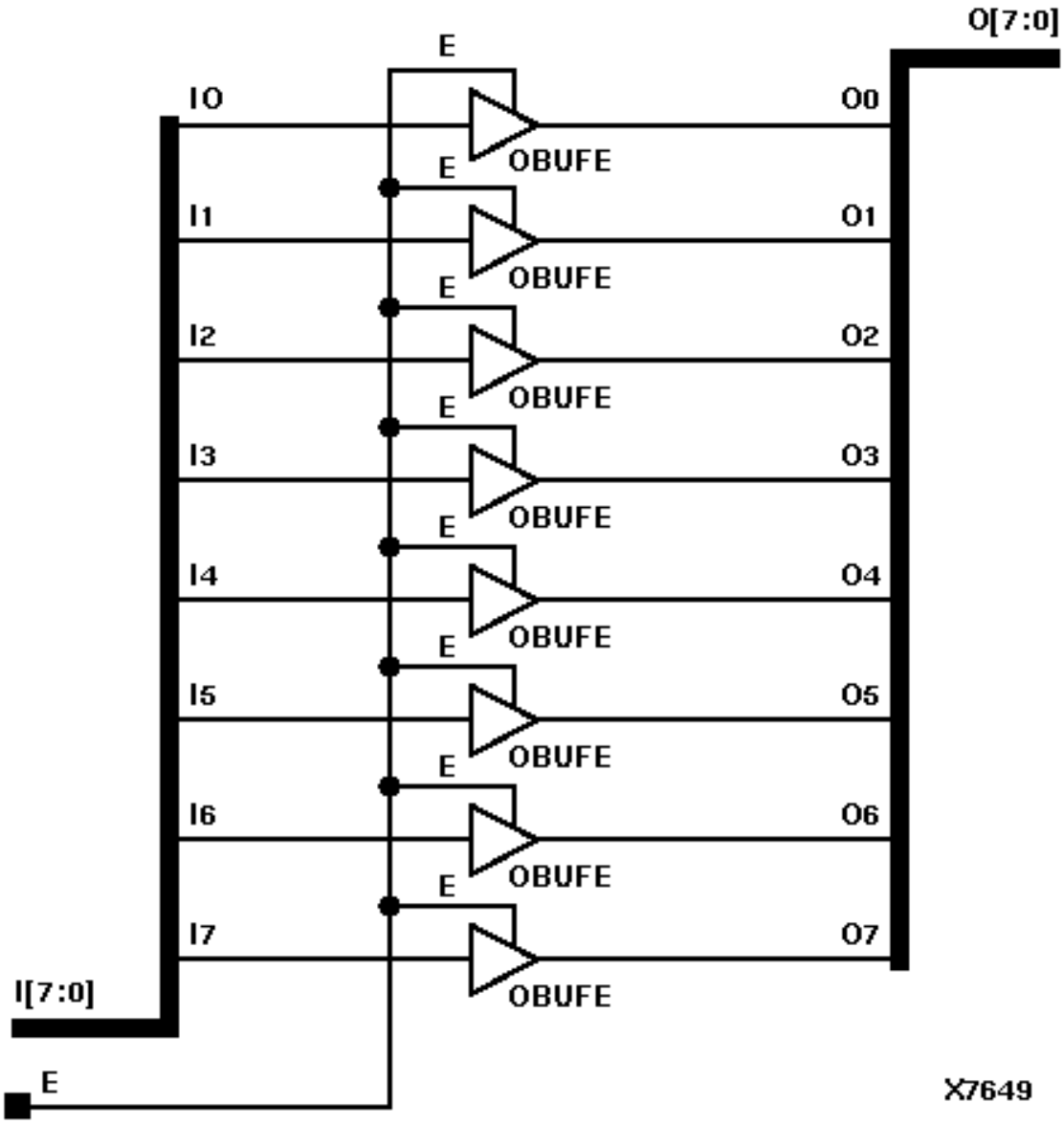


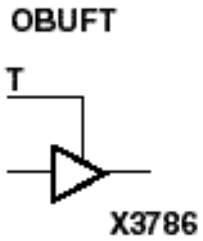
Figure 8-3OBUFE8 Implementation XC3000, XC4000, XC5200, XC9000, Spartans, Virtex

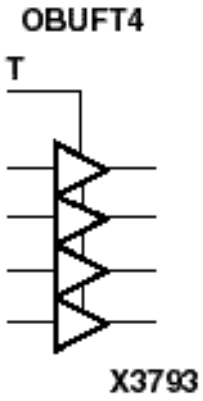


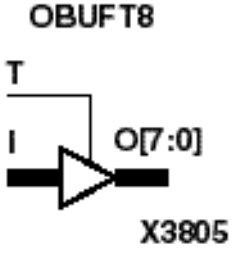
OBUFT, 4, 8, 16

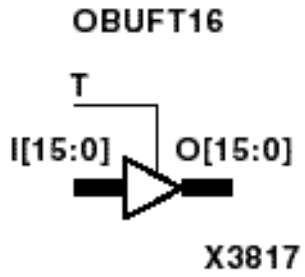
Single and Multiple 3-State Output Buffers with Active-Low Output Enable

Element	XC3000	XC4000E	XC4000X	XC5200	XC9500	Spartan	Spartan XL	Virtex
OBUFT	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
OBUFT4, OBUFT8, OBUFT16	Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro







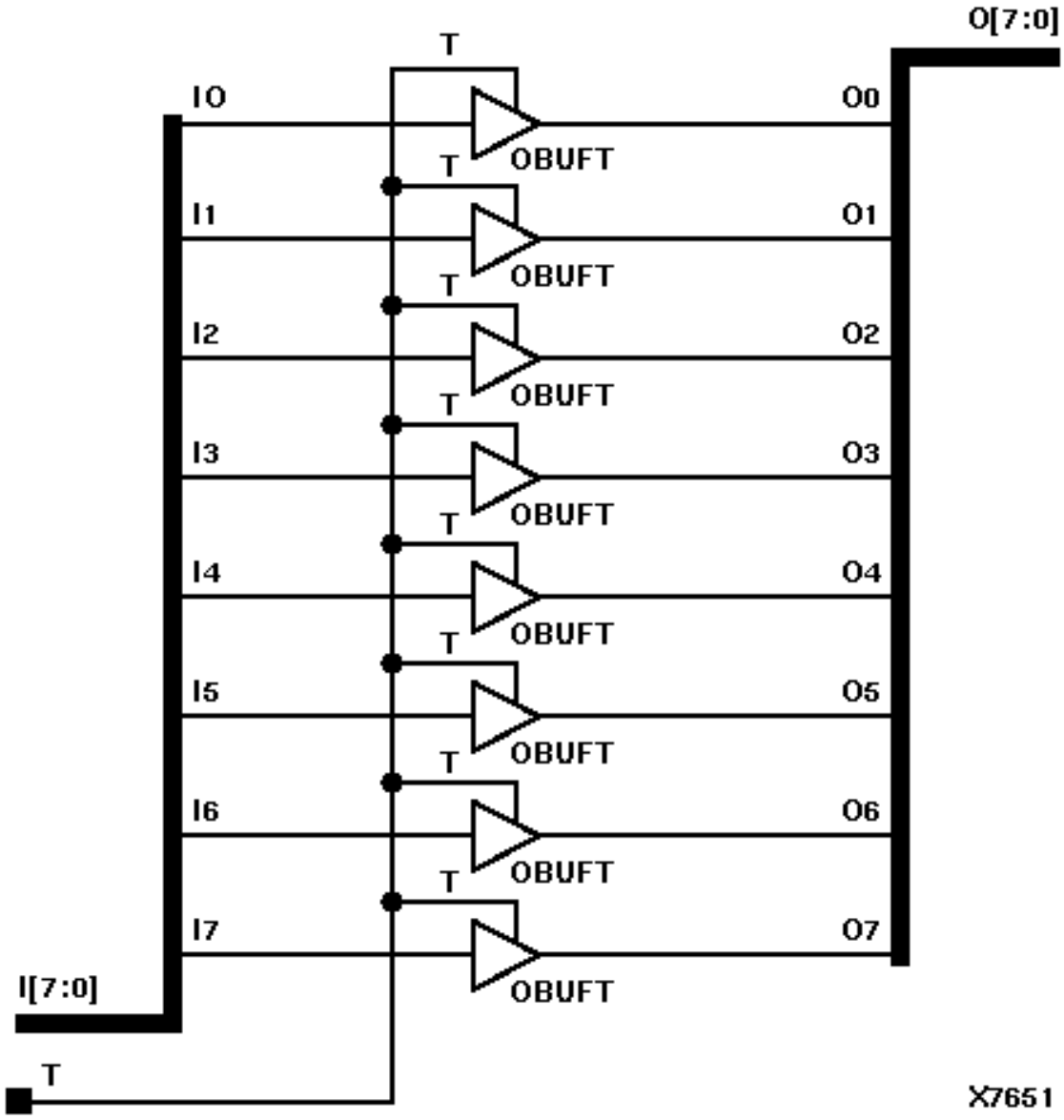


OBUFT, OBUFT4, OBUFT8, and OBUFT16 are single and multiple 3-state output buffers with inputs I, I3 – I0, I7 – I0, I15 – I0, outputs O, O3 – O0, O7 – O0, O15 – O0, and active-Low output enables (T). When T is Low, data on the inputs of the buffers is transferred to the corresponding outputs. When T is High, the output is high impedance (off or Z state). OBUFTs isolate the internal circuit and provide extra drive current for signals leaving a chip. An OBUFT output is connected to an OPAD or an IOPAD.

For Virtex, refer to the **"OBUFT_selectIO"** section for information on OBUFT variants with selectable I/O interfaces. OBUFT, 4, 8, and 16 use the LVTTL standard. Also, Virtex OBUFT, 4, 8, and 16 have selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

Inputs		Outputs
T	**I**	**O**
1	X	Z
0	1	1
0	0	0

Figure 8-4OBUFT8 Implementation XC3000, XC4000, XC5200, XC9000, Spartans, Virtex

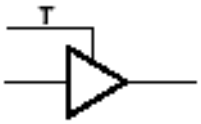


OBUFT_*selectIO*

Single 3-State Output Buffer with Active-Low Output Enable and Selectable I/O Interface

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex

N/A	N/A	N/A	N/A	N/A	N/A	N/A	Primitive



X8720

OBUFT and its variants (listed below) are single 3-state output buffers with active-Low output Enable whose I/O interface corresponds to a specific I/O standard. The name extensions (LVCMOS2, PCI33_3, PCI33_5, etc.) specify the standard. The S, F, and 2, 4, 6, 8, 12, 16, 24 extensions specify the slew rate (SLOW or FAST) and the drive power (2, 4, 6, 8, 12, 16, 24 mA) for the LVTTL standard. For example, OBUFT_S_4 is a 3-state output buffer with active-low output enable that uses the LVTTL I/O signaling standard with a SLOW slew and 4mA of drive power.

OBUFT has selectable drive and slew rates using the DRIVE and FAST or SLOW constraints. The defaults are DRIVE=12 mA and SLOW slew.

When T is Low, data on the input of the buffer is transferred to the output. When T is High, the output is high impedance (off or Z state). OBUFTs isolate the internal circuit and provide extra drive current for signals leaving a chip. An OBUFT output is connected to an OPAD or an IOPAD.

The hardware implementation of the I/O standards requires that you follow a set of usage rules for the SelectI/O buffer components. Refer to the **"SelectI/O Usage Rules" section** under the IBUF_*selectIO* section for information on using these components.

Inputs		**Outputs**
T	**I**	**O**
1	X	Z
0	1	1
0	0	0

Component	**I/O Standard**	**VCCO**
OBUFT	LVTTL	3.3
OBUFT_S_2	LVTTL	3.3
OBUFT_S_4	LVTTL	3.3
OBUFT_S_6	LVTTL	3.3
OBUFT_S_8	LVTTL	3.3

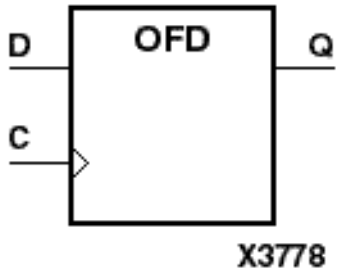
OBUFT_S_12	LVTTL	3.3
OBUFT_S_16	LVTTL	3.3
OBUFT_S_24	LVTTL	3.3
OBUFT_F_2	LVTTL	3.3
OBUFT_F_4	LVTTL	3.3
OBUFT_F_6	LVTTL	3.3
OBUFT_F_8	LVTTL	3.3
OBUFT_F_12	LVTTL	3.3
OBUFT_F_16	LVTTL	3.3
OBUFT_F_24	LVTTL	3.3
OBUFT_LVCMOS2	LVCMOS2	2.5
OBUFT_PCI33_3	PCI33_3	3.3
OBUFT_PCI33_5	PCI33_5	3.3
OBUFT_PCI66_3	PCI66_3	3.3
OBUFT_GTL	GTL	N/A
OBUFT_GTLP	GTL+	N/A
OBUFT_HSTL_I	HSTL_I	1.5
OBUFT_HSTL_III	HSTL_III	1.5
OBUF_HSTL_IV	HSTL_IV	1.5
OBUFT_SSTL2_I	SSTL2_I	2.5
OBUFT_SSTL2_II	SSTL2_II	2.5
OBUFT_SSTL3_I	SSTL3_I	3.3
OBUFT_SSTL3_II	SSTL3_II	3.3
OBUFT_CTT	CTT	3.3
OBUFT_AGP	AGP	3.3

OFD, 4, 8, 16

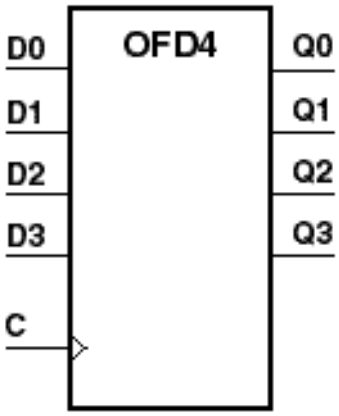
Single- and Multiple-Output D Flip-Flops

Eleme	XC300	XC400	XC400	XC520	XC900	Sparta	Spartan	Virtex

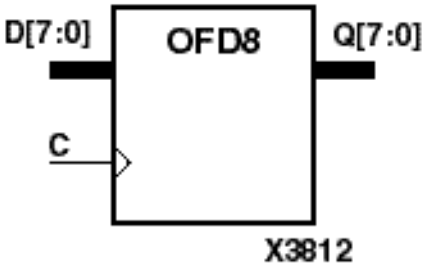
nt	0	0E	0X	0	0	n	XL	
OFD	Primitive	Macro	Macro	Macro	Macro	Macro	Macro	Macro
OFD4, OFD8, OFD16	Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro



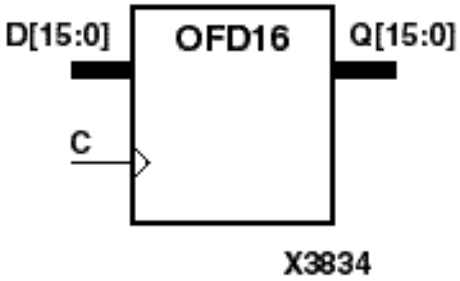
X3778



X3800



X3812



OFD, OFD4, OFD8, and OFD16 are single and multiple output D flip-flops except for XC5200 and XC9000. The flip-flops exist in an input/output block (IOB) for XC3000, XC4000, and Spartans. The outputs (for example, Q3 – Q0) are connected to OPADs or IOPADs. The data on the D inputs is loaded into the flip-flops during the Low-to-High clock (C) transition and appears on the Q outputs.

The flip-flops are asynchronously cleared with Low outputs when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs		Outputs
D	**C**	**Q**
D	↑	dn

dn = state of referenced input one setup time prior to active clock transition

Figure 8-5OFD Implementation XC4000, Spartans

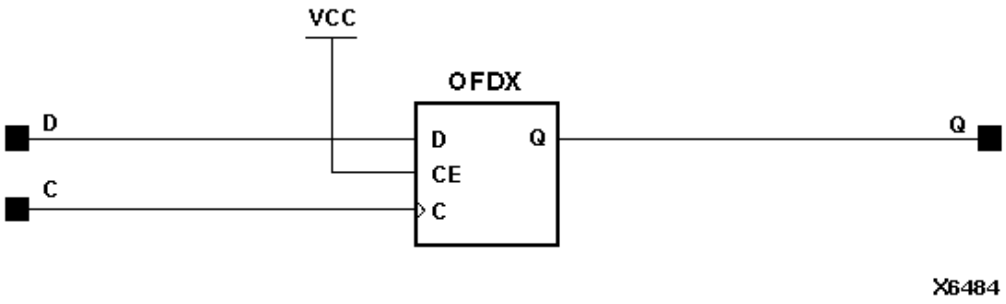


Figure 8-6OFD Implementation XC5200, Virtex

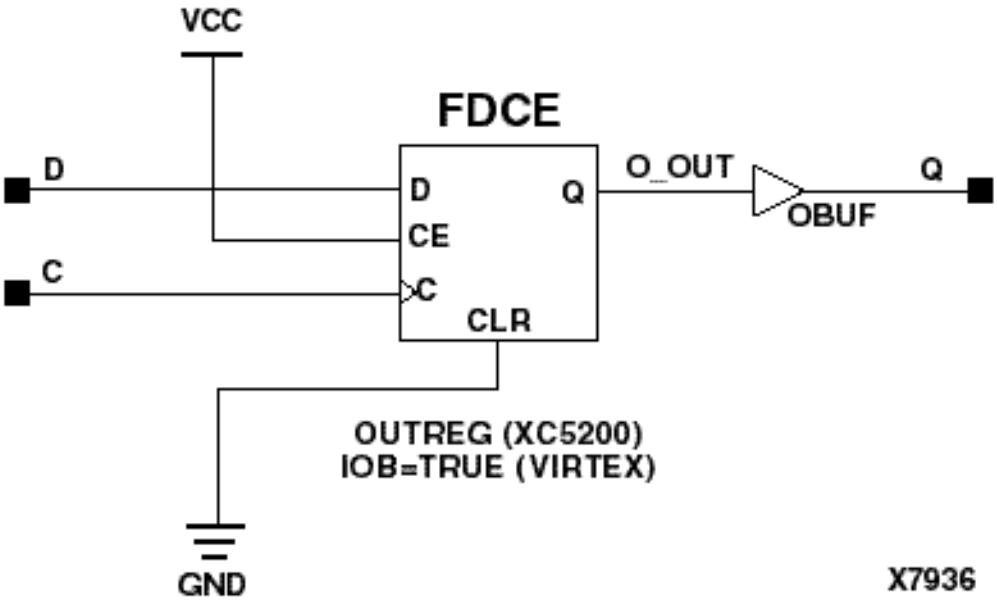


Figure 8-7OFD Implementation XC9000

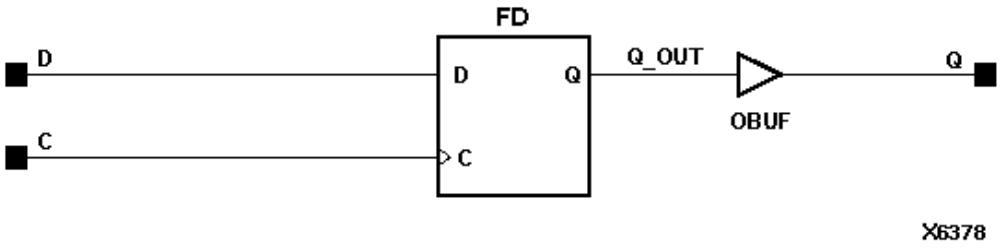


Figure 8-8OFD8 Implementation XC3000, XC4000, XC5200, Spartans, Virtex

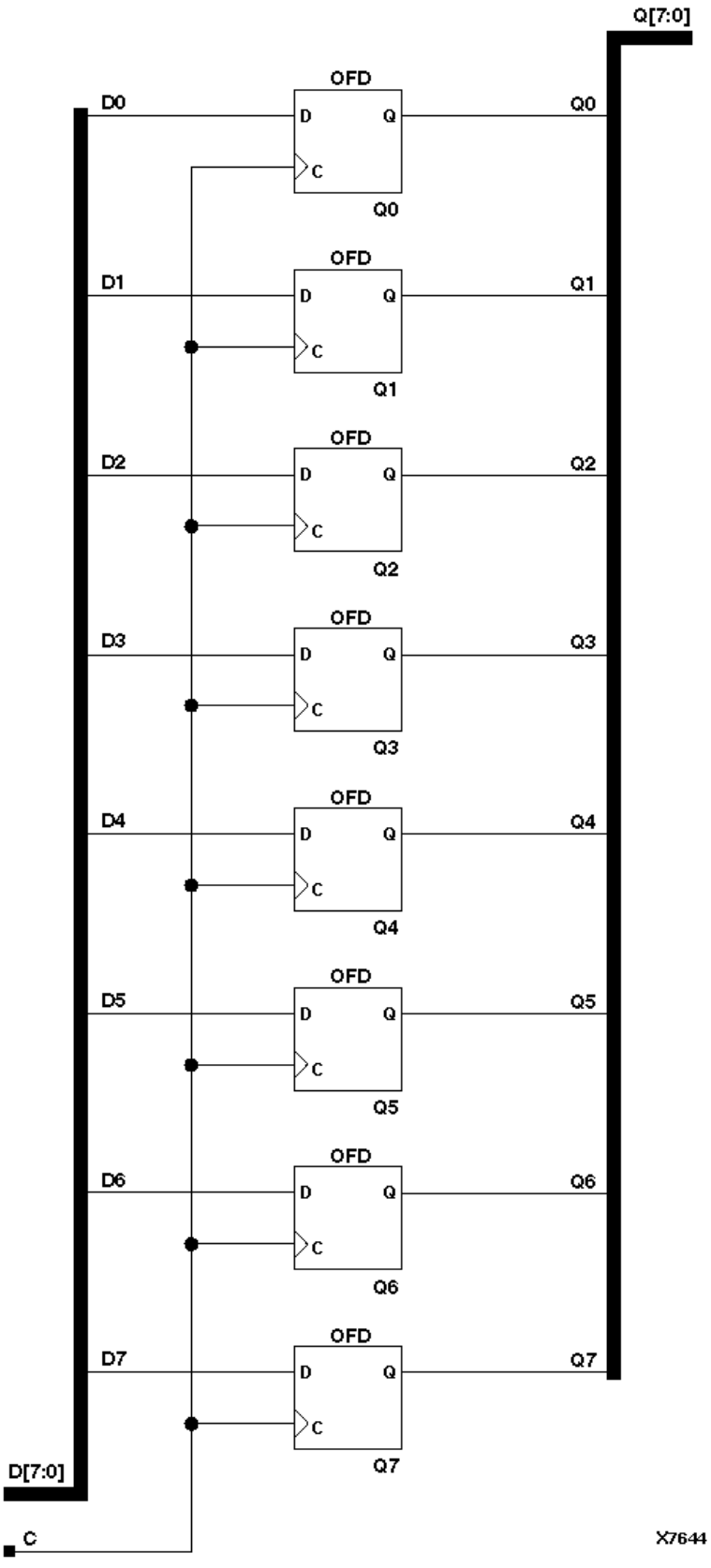
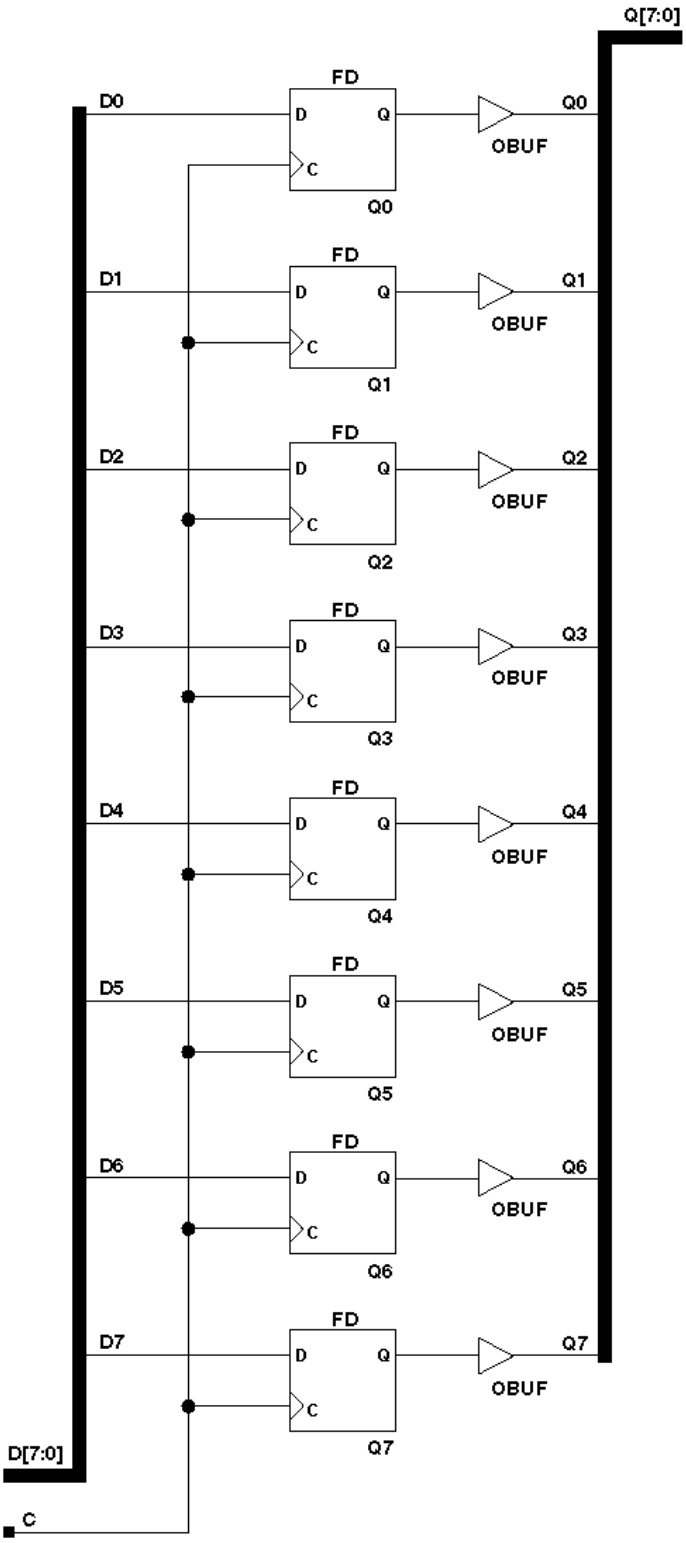

Q[7:0]
OFD
D0
D
Q
Q0
C
Q0
D1
Q1
Q1
D2
Q2
Q2
D3
Q3
Q3
D4
Q4
Q4
D5
Q5
Q5
D6
Q6
Q6
D7
Q7
Q7
D[7:0]
C
X7644

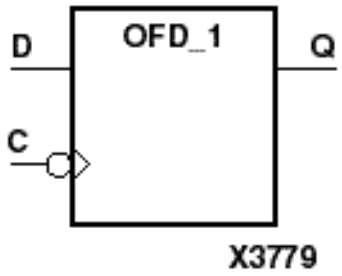
Figure 8-9OFD8 Implementation XC9000


Q[7:0]
FD
D0
D
Q
Q0
OBUF
C
Q0
D1
Q1
Q1
D2
Q2
Q2
D3
Q3
Q3
D4
Q4
Q4
D5
Q5
Q5
D6
Q6
Q6
D7
Q7
Q7
D[7:0]
C
X7648

OFD_1

Output D Flip-Flop with Inverted Clock

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	N/A	Macro	Macro	Macro



OFD_1 is located in an input/output block (IOB) except for XC5200. The output (Q) of the D flip-flop is connected to an OPAD or an IOPAD. The data on the D input is loaded into the flip-flop during the High-to-Low clock (C) transition and appears on the Q output.

The flip-flop is asynchronously cleared, output Low, when power is applied. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs		Outputs
D	**C**	**Q**
D	↓	d

d = state of referenced input one setup time prior to active clock transition

Figure 8-10OFD_1 Implementation XC3000, XC4000, Spartans

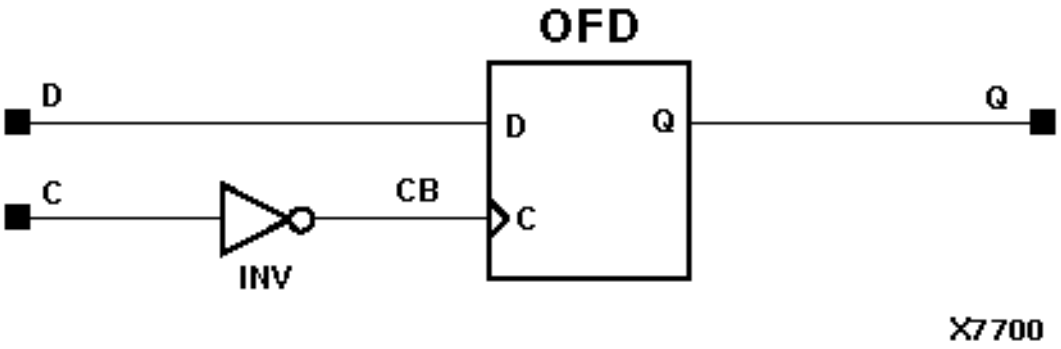
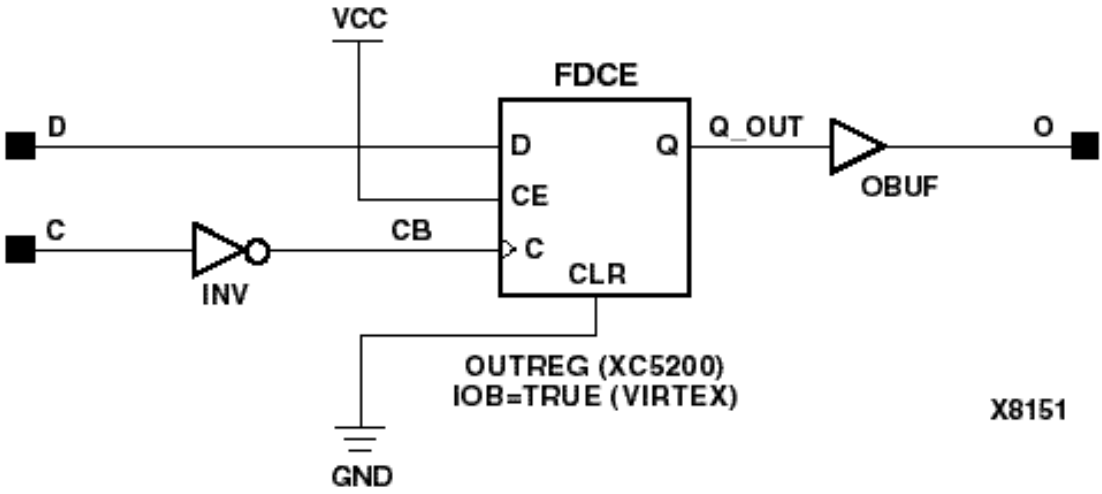


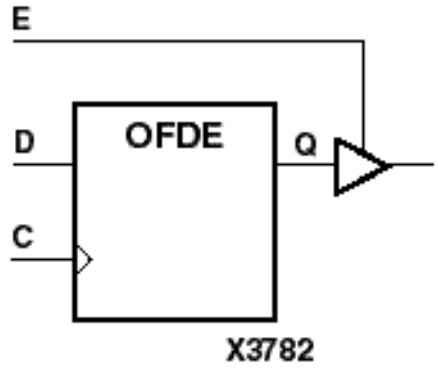
Figure 8-11OFD_1 Implementation XC5200, Virtex

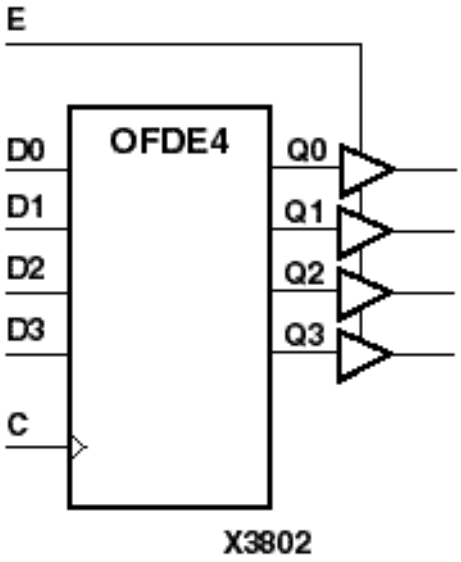


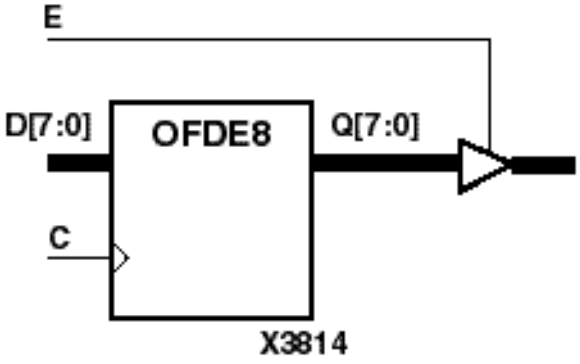
OFDE, 4, 8, 16

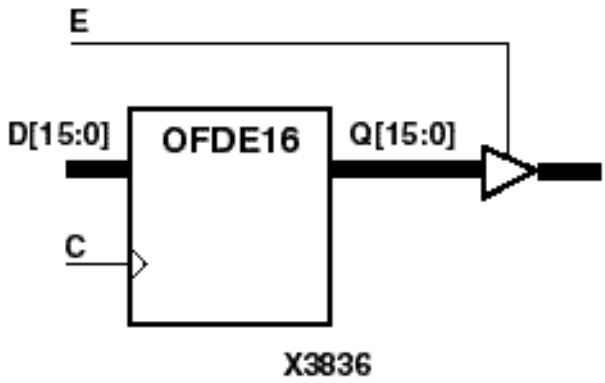
D Flip-Flops with Active-High Enable Output Buffers

Element	XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	Spartan XL	Virtex
OFDE	Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro
OFDE4, OFDE8, OFDE16	Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro


E
D
OFDE
Q
C
X3782


E
D0
OFDE4
Q0
D1
Q1
D2
Q2
D3
Q3
C
X3802


E
D[7:0]
OFDE8
Q[7:0]
C
X3814



OFDE, OFDE4, OFDE8, and OFDE16 are single or multiple D flip-flops whose outputs are enabled by tristate buffers. The flip-flop data outputs (Q) are connected to the inputs of output buffers (OBUFE). The OBUFE outputs (O) are connected to OPADs or IOPADs. These flip-flops and buffers are contained in input/output blocks (IOB) for XC3000 and XC4000. The data on the data inputs (D) is loaded into the flip-flops during the Low-to-High clock (C) transition. When the active-High enable inputs (E) are High, the data on the flip-flop outputs (Q) appears on the O outputs. When E is Low, outputs are high impedance (Z state or Off).

The flip-flops are asynchronously cleared with Low outputs when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs			Outputs
E	**D**	**C**	**O**
0	X	X	Z, not off
1	1	↑	1
1	0	↑	0

Figure 8-12OFDE Implementation XC3000, XC4000, Spartans

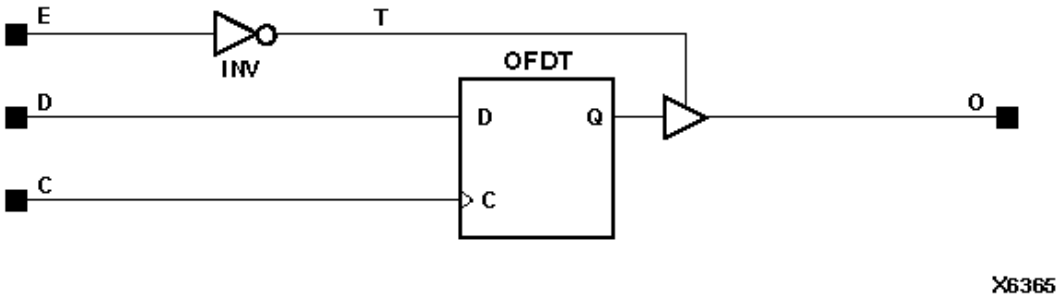


Figure 8-13OFDE Implementation XC5200, Virtex

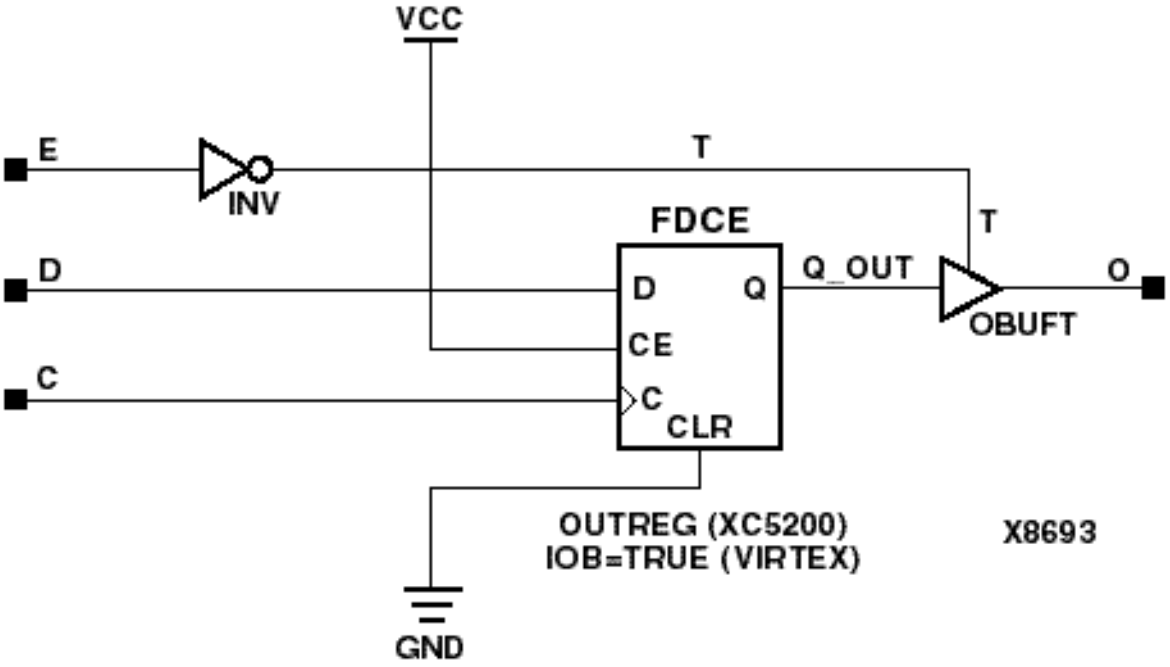


Figure 8-14OFDE Implementation XC9000

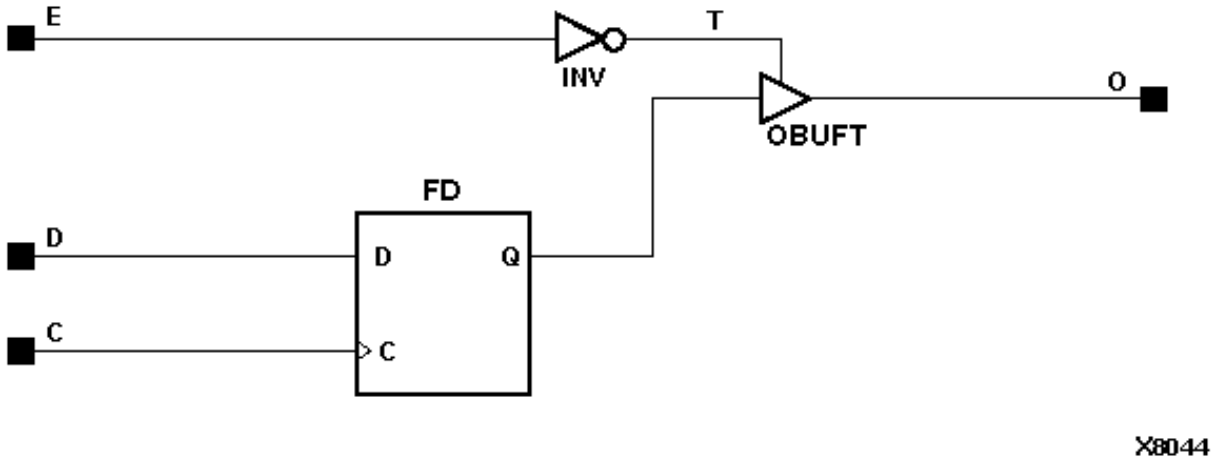
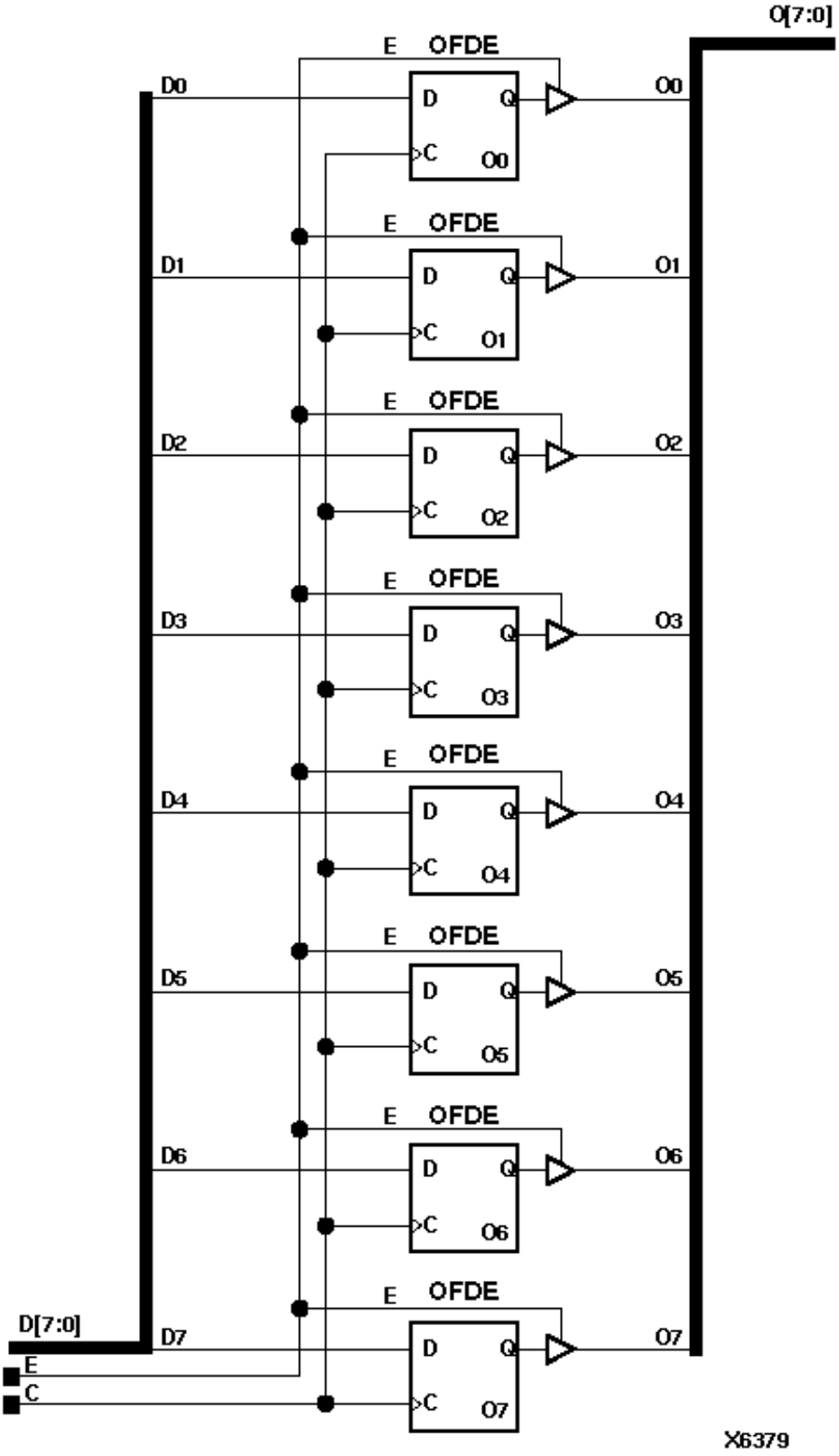


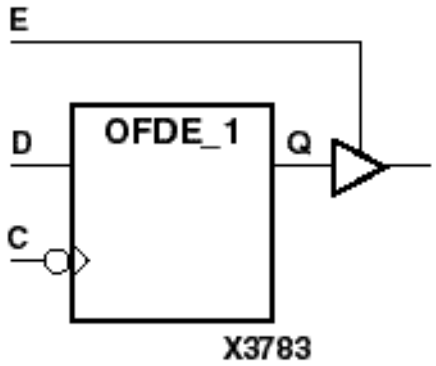
Figure 8-15OFDE8 Implementation XC3000, XC4000, XC5200, XC9000, Spartans, Virtex


O[7:0]
E
OFDE
D0
D
Q
O0
C
O0
D1
O1
O1
D2
O2
O2
D3
O3
O3
D4
O4
O4
D5
O5
O5
D6
O6
O6
D7
O7
O7
D[7:0]
E
C
X6379

OFDE_1

D Flip-Flop with Active-High Enable Output Buffer and Inverted Clock

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	N/A	Macro	Macro	Macro



OFDE_1 and its output buffer are located in an input/output block (IOB) except for XC5200. The data output of the flip-flop (Q) is connected to the input of an output buffer or OBUFE. The output of the OBUFE is connected to an OPAD or an IOPAD. The data on the data input (D) is loaded into the flip-flop on the High-to-Low clock (C) transition. When the active-High enable input (E) is High, the data on the flip-flop output (Q) appears on the O output. When E is Low, the output is high impedance (Z state or Off).

The flip-flop is asynchronously cleared with Low output when power is applied. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs			Outputs
E	**D**	**C**	**O**
0	X	X	Z
1	1	↓	1
1	0	↓	0

Figure 8-16OFDE_1 Implementation XC3000, XC4000, Spartans

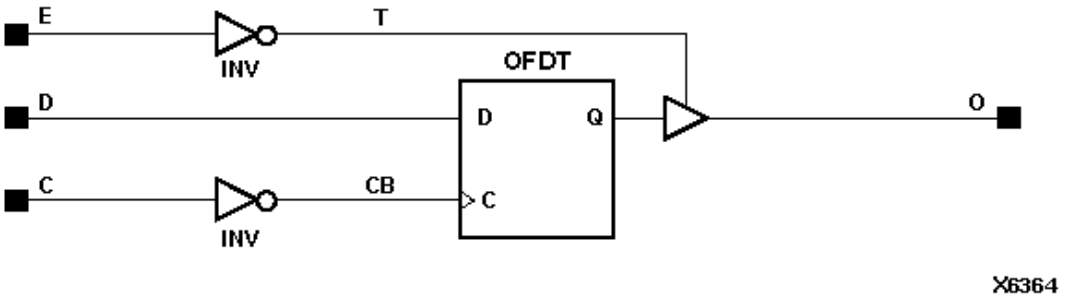
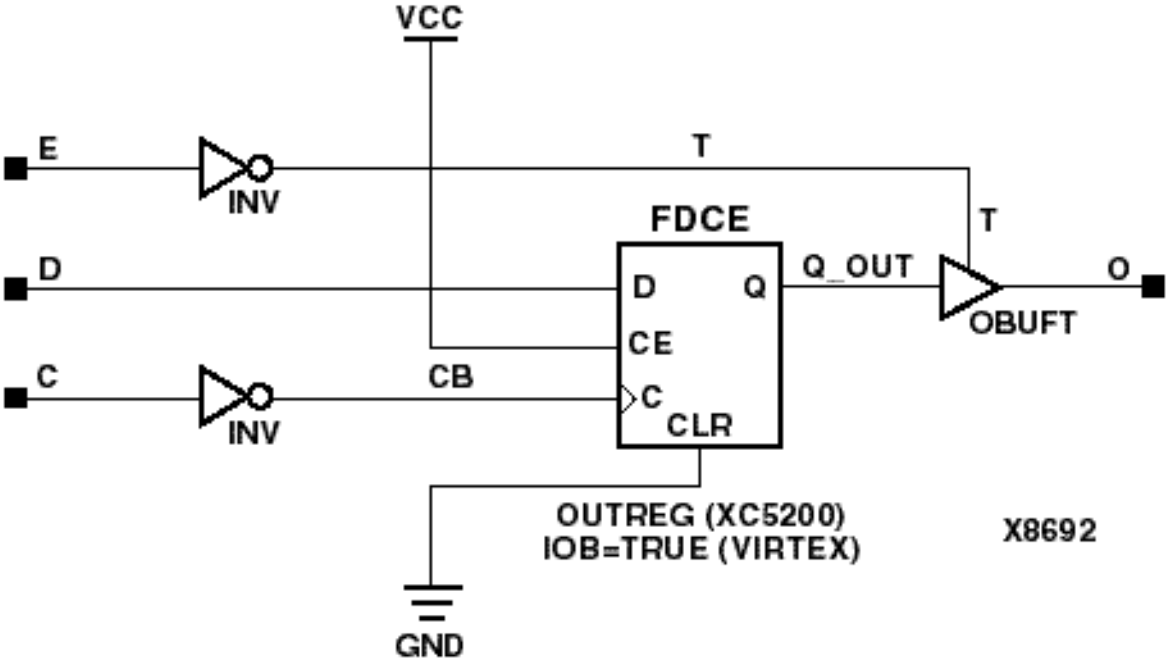


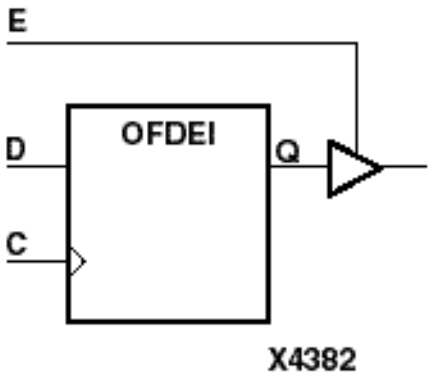
Figure 8-17OFDE_1 Implementation XC5200, Virtex



OFDEI

D Flip-Flop with Active-High Enable Output Buffer (Asynchronous Preset)

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	N/A	N/A	Macro	Macro	N/A

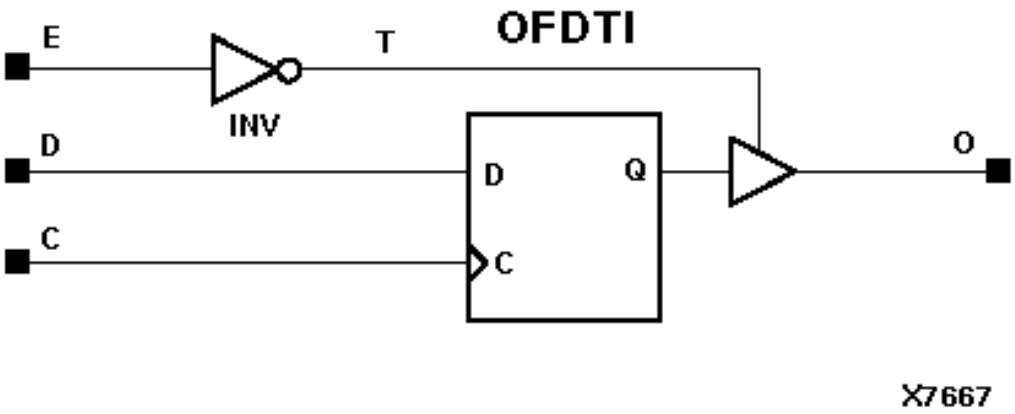


OFDEI is a D flip-flop whose output is enabled by a 3-state buffer. The data output (Q) of the flip-flop is connected to the input of an output 3-state buffer or OBUFE. The output of the OBUFE (O) is connected to an OPAD or an IOPAD. These flip-flops and buffers are contained in input/output blocks (IOB). The data on the data input (D) is loaded into the flip-flop during the Low-to-High clock (C) transition. When the active-High enable input (E) is High, the data on the flip-flop output (Q) appears on the O output. When E is Low, the output is high impedance (Z state or off).

The flip-flop is asynchronously preset, output High, when power is applied. FPGAs simulate power-on when global set/reset (GSR) is active. GSR (XC4000, Spartans) default to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP symbol.

Inputs			Outputs
E	**D**	**C**	**O**
0	X	X	Z
1	1	↑	1
1	0	↑	0

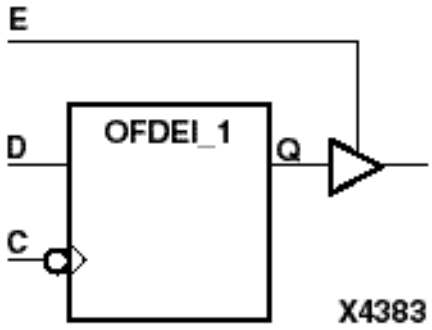
Figure 8-18OFDEI Implementation XC4000, Spartans



OFDEI_1

D Flip-Flop with Active-High Enable Output Buffer and Inverted Clock (Asynchronous Preset)

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	N/A	N/A	Macro	Macro	N/A



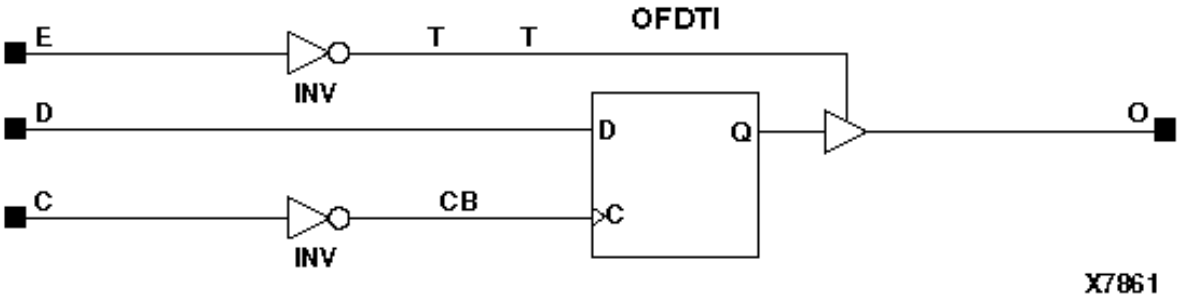
OFDEI_1 and its output buffer exist in an input/output block (IOB). The data output of the flip-flop (Q) is connected to the input of an output buffer or OBUFE. The output of the OBUFE is connected to an OPAD or an IOPAD. The data on the data input (D) is loaded into the flip-flop on the High-to-Low clock (C) transition. When the active-High enable input (E) is High, the data on the flip-flop output (Q) appears on the O output. When E is Low, the output is high impedance (Z state or off).

The flip-flop is asynchronously preset, output High, when power is applied. FPGAs simulate power-on when global

set/reset (GSR) is active. GSR (XC4000, Spartans) default to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP symbol.

Inputs			Outputs
E	**D**	**C**	**O**
0	X	X	Z
1	1	↓	1
1	0	↓	0

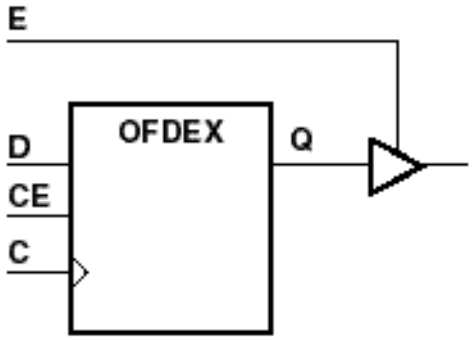
Figure 8-19OFDEI_1 Implementation XC4000, Spartans



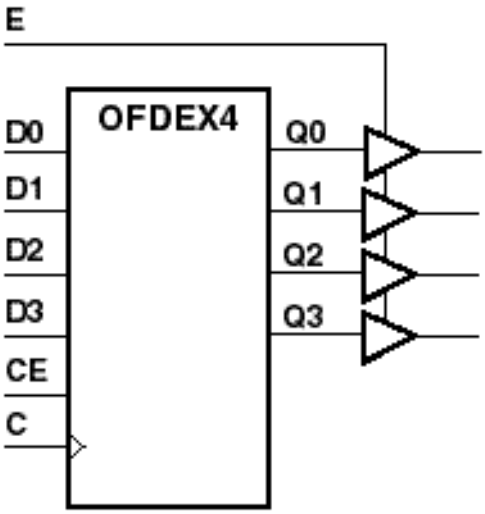
OFDEX, 4, 8, 16

D Flip-Flops with Active-High Enable Output Buffers and Clock Enable

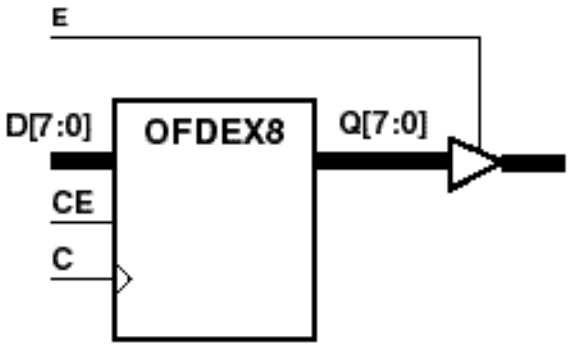
XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	N/A	N/A	Macro	Macro	N/A



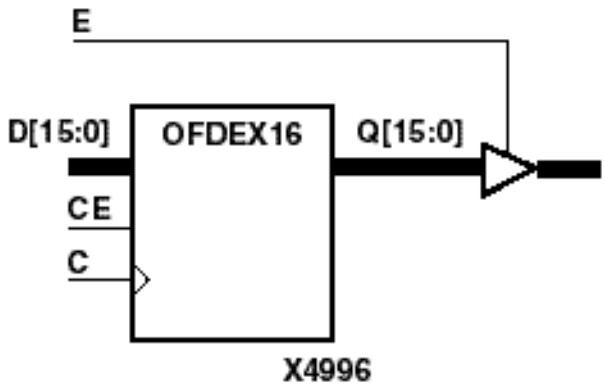
X4993



X4994



X4995



OFDEX, OFDEX4, OFDEX8, and OFDEX16 are single or multiple D flip-flops whose outputs are enabled by tristate buffers. The flip-flop data outputs (Q) are connected to the inputs of output buffers (OBUFE). The OBUFE outputs (O) are connected to OPADs or IOPADs. These flip-flops and buffers are contained in input/output blocks (IOB). The data on the data inputs (D) is loaded into the flip-flops during the Low-to-High clock (C) transition. When the active-High enable inputs (E) are High, the data on the flip-flop outputs (Q) appears on the O outputs. When E is Low, outputs are high impedance (Z state or Off). When CE is Low and E is High, the outputs do not change.

The flip-flops are asynchronously cleared with Low outputs when power is applied. FPGAs simulate power-on when global set/reset (GSR) is active. GSR (XC4000, Spartans) default to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP symbol.

Inputs				**Outputs**
CE	**E**	**D**	**C**	**O**
X	0	X	X	Z, not off
1	1	1	↑	1
1	1	0	↑	0
0	1	X	X	No Chg

Figure 8-20OFDEX Implementation XC4000, Spartans

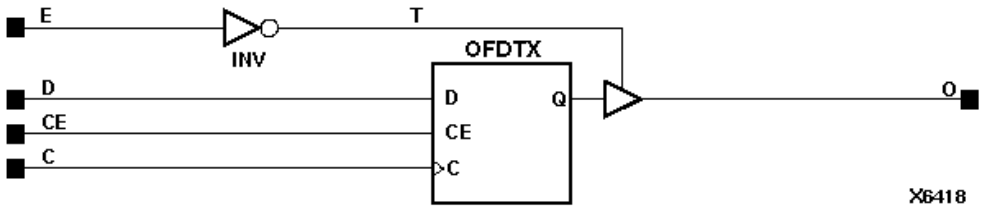
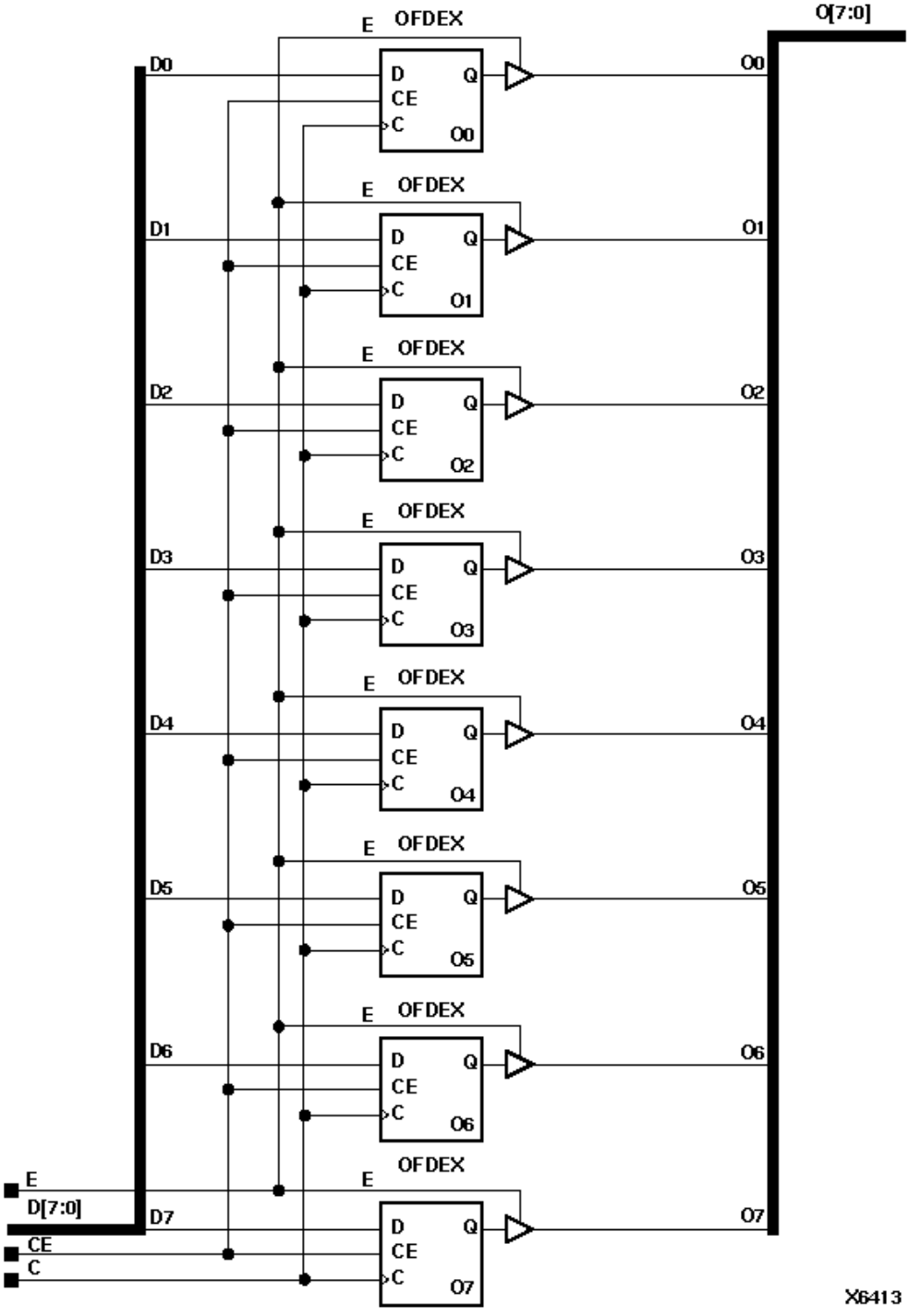


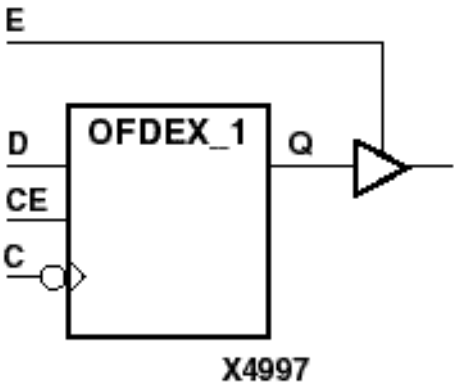
Figure 8-21OFDEX8 Implementation XC4000, Spartans


E
OFDEX
O[7:0]
D0
D
Q
CE
C
O0
O0
D1
O1
O1
D2
O2
O2
D3
O3
O3
D4
O4
O4
D5
O5
O5
D6
O6
O6
D7
O7
O7
E
D[7:0]
CE
C
X6413

OFDEX_1

D Flip-Flop with Active-High Enable Output Buffer, Inverted Clock, and Clock Enable

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	N/A	N/A	Macro	Macro	N/A

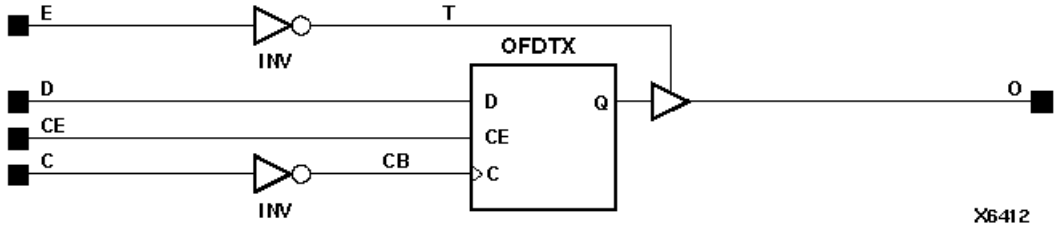


OFDEX_1 and its output buffer are located in an input/output block (IOB). The data output of the flip-flop (Q) is connected to the input of an output buffer or OBUFE. The output of the OBUFE is connected to an OPAD or an IOPAD. The data on the data input (D) is loaded into the flip-flop on the High-to-Low clock (C) transition. When the active-High enable input (E) is High, the data on the flip-flop output (Q) appears on the O output. When E is Low, the output is high impedance (Z state or Off). When CE is Low and E is High, the output does not change.

The flip-flop is asynchronously cleared with Low output when power is applied. FPGAs simulate power-on when global set/reset (GSR) is active. GSR (XC4000, Spartans) default to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP symbol.

Inputs				Outputs
CE	**E**	**D**	**C**	**O**
X	0	X	X	Z
1	1	1	↓	1
1	1	0	↓	0
0	1	X	X	No Chg

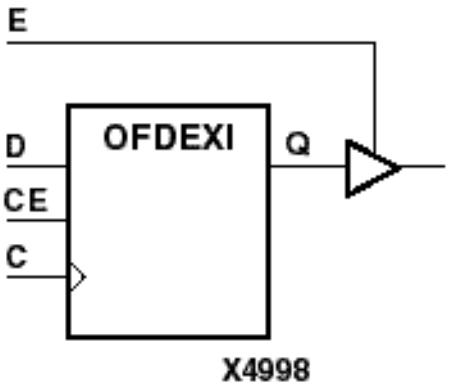
Figure 8-22OFDEX_1 Implementation XC4000, Spartans



OFDEXI

D Flip-Flop with Active-High Enable Output Buffer and Clock Enable (Asynchronous Preset)

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	N/A	N/A	Macro	Macro	N/A

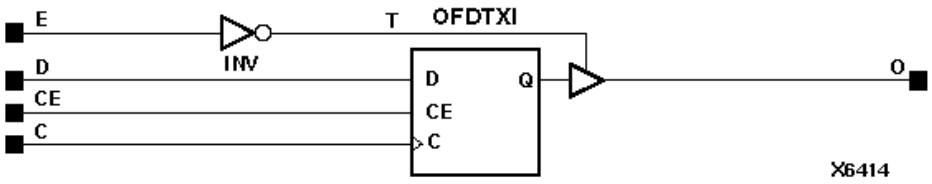


OFDEXI is a D flip-flop whose output is enabled by a tristate buffer. The data output (Q) of the flip-flop is connected to the input of an output buffer or OBUFE. The output of the OBUFE (O) is connected to an OPAD or an IOPAD. These flip-flops and buffers are contained in input/output blocks (IOB). The data on the data input (D) is loaded into the flip-flop during the Low-to-High clock (C) transition. When the active-High enable input (E) is High, the data on the flip-flop output (Q) appears on the O output. When E is Low, the output is high impedance (Z state or Off). When CE is Low and E is High, the output does not change.

The flip-flop is asynchronously preset, output High, when power is applied. FPGAs simulate power-on when global set/reset (GSR) is active. GSR (XC4000, Spartans) default to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP symbol.

Inputs				Outputs
CE	**E**	**D**	**C**	**O**
X	0	X	X	Z
1	1	1	↑	1
1	1	0	↑	0
0	1	X	X	No Chg

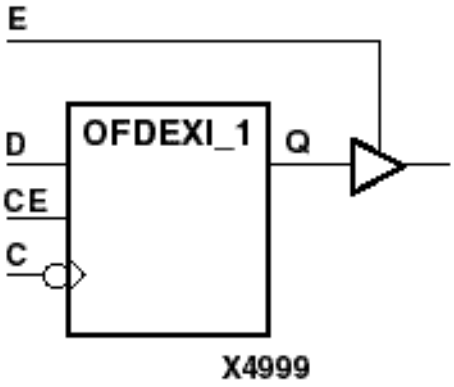
Figure 8-23OFDEXI Implementation XC4000, Spartans



OFDEXI_1

D Flip-Flop with Active-High Enable Output Buffer, Inverted Clock, and Clock Enable (Asynchronous Preset)

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	N/A	N/A	Macro	Macro	N/A

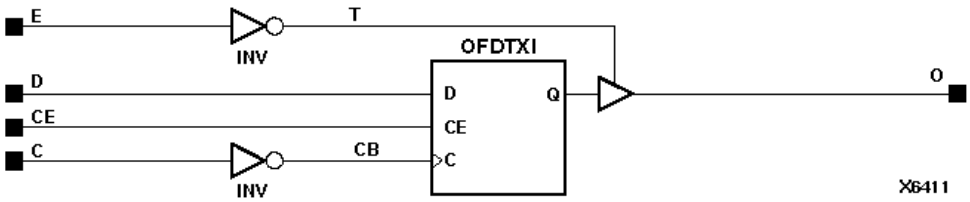


OFDEXI_1 and its output buffer are located in an input/output block (IOB). The data output of the flip-flop (Q) is connected to the input of an output buffer or OBUFE. The output of the OBUFE is connected to an OPAD or an IOPAD. The data on the data input (D) is loaded into the flip-flop on the High-to-Low clock (C) transition. When the active-High enable input (E) is High, the data on the flip-flop output (Q) appears on the O output. When E is Low, the output is high impedance (Z state or Off). When CE is Low and E is High, the output does not change.

The flip-flop is asynchronously preset, output High, when power is applied. FPGAs simulate power-on when global set/reset (GSR) is active. GSR (XC4000, Spartans) default to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP symbol.

Inputs				**Outputs**
CE	**E**	**D**	**C**	**O**
X	0	X	X	Z
1	1	1	↓	1
1	1	0	↓	0
0	1	X	X	No Chg

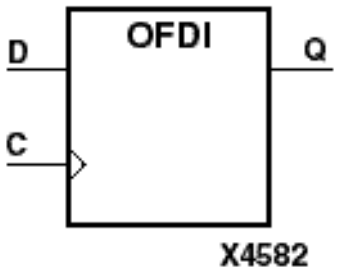
Figure 8-24OFDEXI_1 Implementation XC4000, Spartans



OFDI

Output D Flip-Flop (Asynchronous Preset)

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	N/A	N/A	Macro	Macro	Macro



OFDI is contained in an input/output block (IOB). The output (Q) of the D flip-flop is connected to an OPAD or an IOPAD. The data on the D input is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q).

The flip-flop is asynchronously preset, output High, when power is applied. FPGAs simulate power-on when global set/reset (GSR) is active. GSR (XC4000, Spartans) default to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP symbol.

Inputs		Outputs
D	C	Q

D	↑	d

d = state of referenced input one setup time prior to active clock transition

Figure 8-25OFDI Implementation XC4000, Spartans

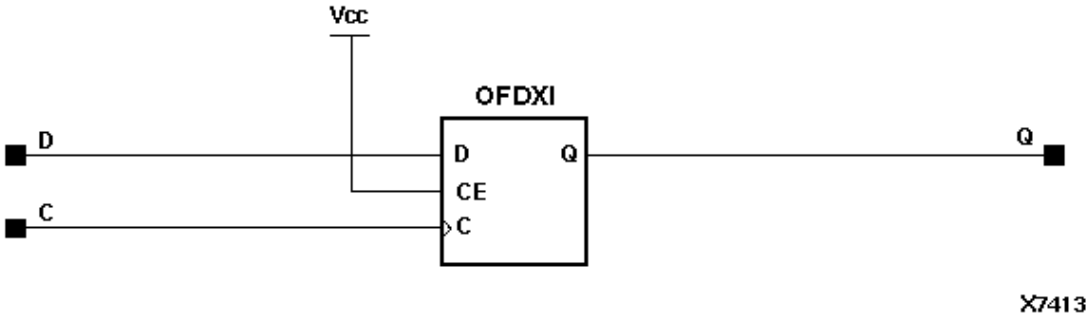
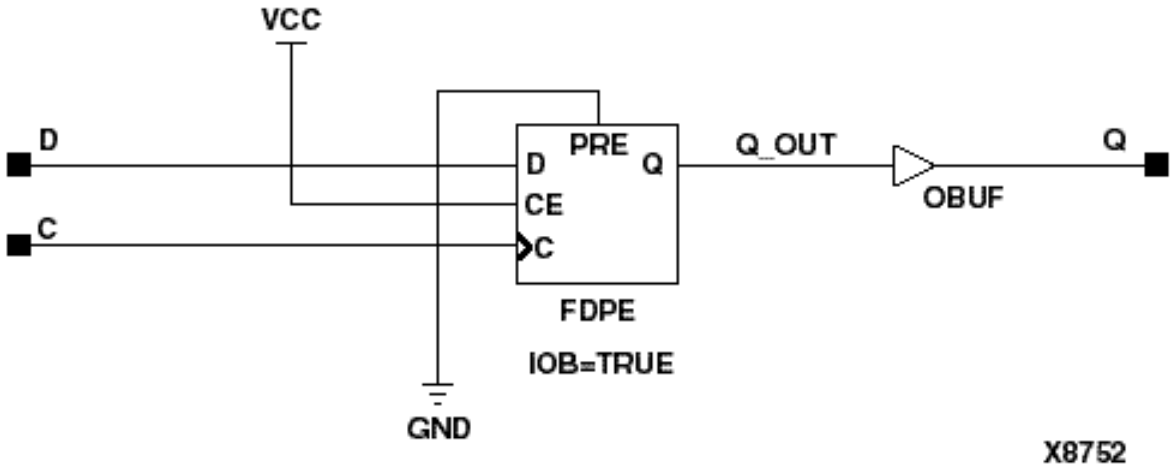


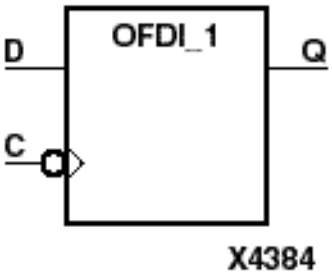
Figure 8-26OFDI Implementation Virtex



OFDI_1

Output D Flip-Flop with Inverted Clock (Asynchronous Preset)

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	N/A	N/A	Macro	Macro	Macro



OFDI_1 exists in an input/output block (IOB). The D flip-flop output (Q) is connected to an OPAD or an IOPAD. The data on the D input is loaded into the flip-flop during the High-to-Low clock (C) transition and appears on the Q output.

The flip-flop is asynchronously preset, output High, when power is applied. FPGAs simulate power-on when global set/reset (GSR) is active. GSR (XC4000, Spartans) default to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP symbol.

Inputs		Outputs
D	**C**	**Q**
D	↓	d

d = state of referenced input one setup time prior to the active clock transition

Figure 8-27OFDI_1 Implementation XC4000, Spartans

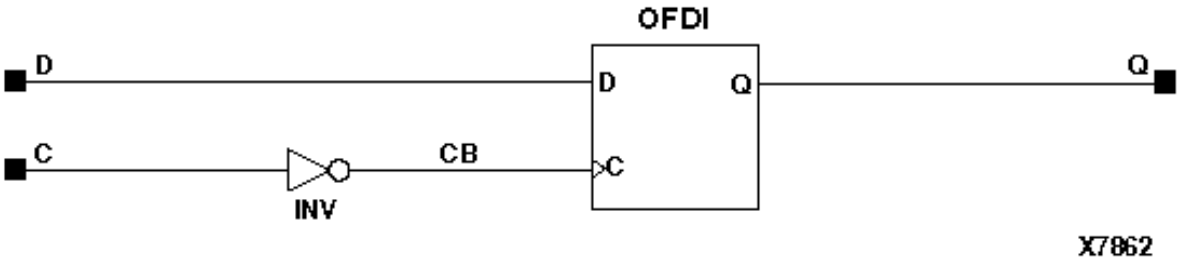
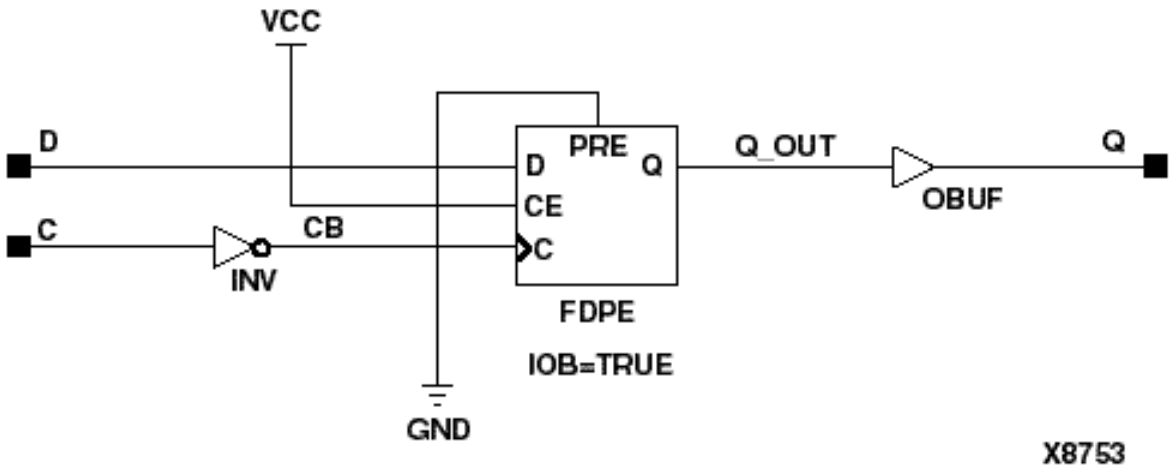


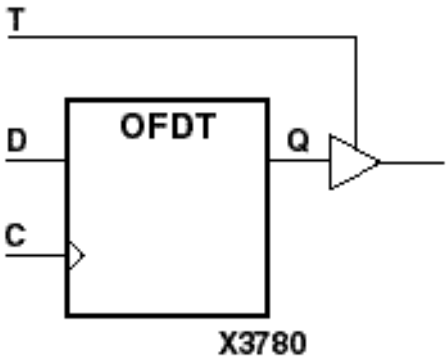
Figure 8-28OFDI_1 Implementation Virtex

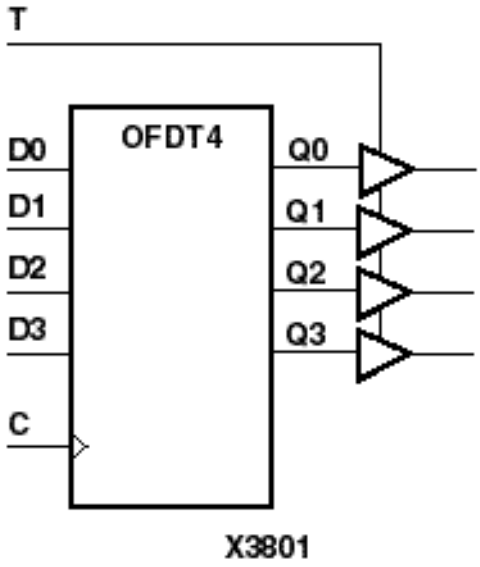


OFDT, 4, 8, 16

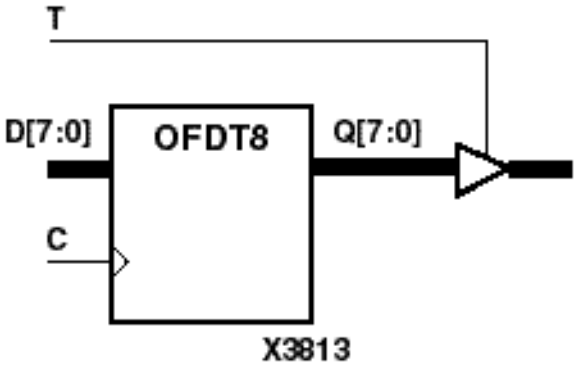
Single and Multiple D Flip-Flops with Active-Low 3-State Output Enable Buffers

Element	XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	Spartan XL	Virtex
OFDT	Primitive	Macro	Macro	Macro	Macro	Macro	Macro	Macro
OFDT4, OFDT8, OFDT16	Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro

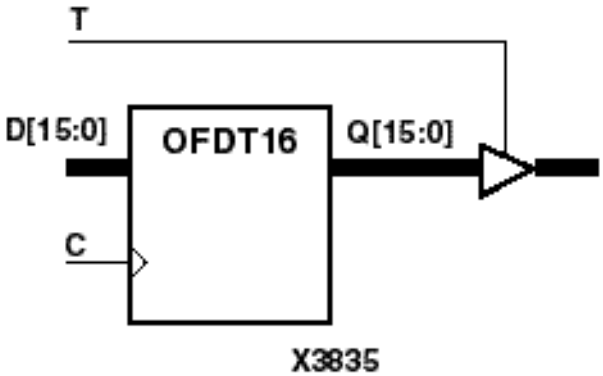




X3801



X3813



X3835

OFDT, OFDT4, OFDT8, and OFDT16 are single or multiple D flip-flops whose outputs are enabled by a tristate buffers. The data outputs (Q) of the flip-flops are connected to the inputs of output buffers (OBUFT). The outputs of the OBUFTs (O) are connected to OPADs or IOPADs. These flip-flops and buffers are located in input/output blocks (IOB) for XC3000 and XC4000. The data on the data inputs (D) is loaded into the flip-flops during the Low-to-High clock (C) transition. When the active-Low enable inputs (T) are Low, the data on the flip-flop outputs (Q) appears on the O outputs. When T is High, outputs are high impedance (Off).

The flip-flops are asynchronously cleared with Low outputs, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when

global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs			Outputs
T	**D**	**C**	**O**
1	X	X	Z
0	D	↑	d

d = state of referenced input one setup time prior to active clock transition

Figure 8-29OFDT Implementation XC4000, Spartans

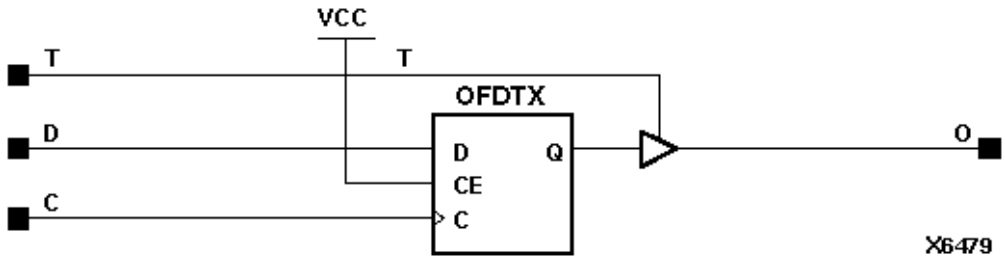


Figure 8-30OFDT Implementation XC5200, Virtex

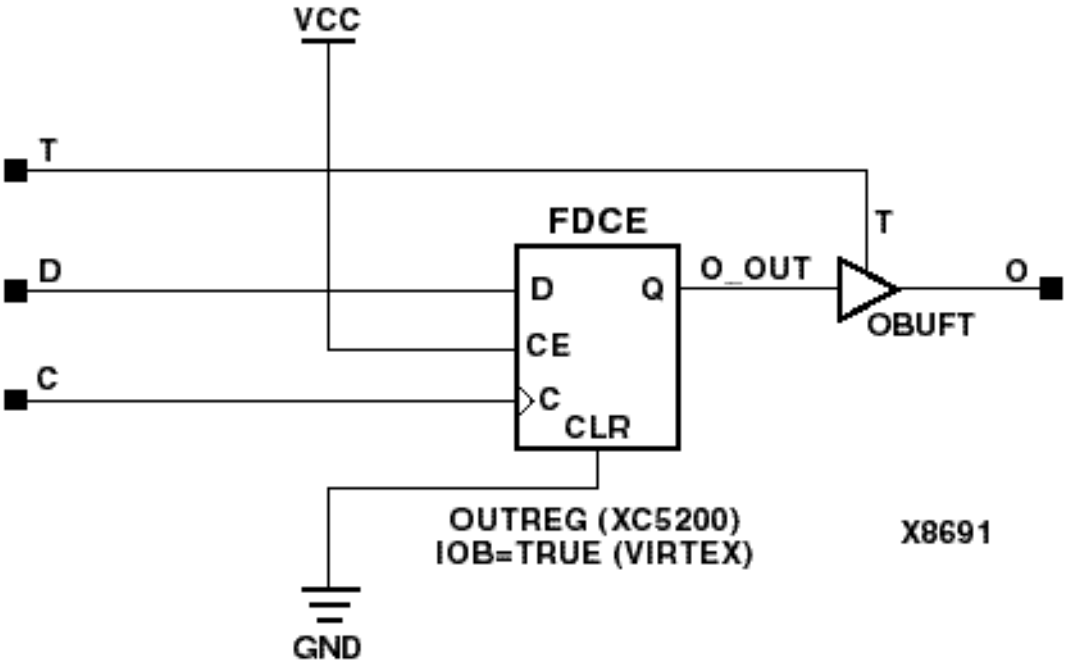


Figure 8-31OFDT Implementation XC9000

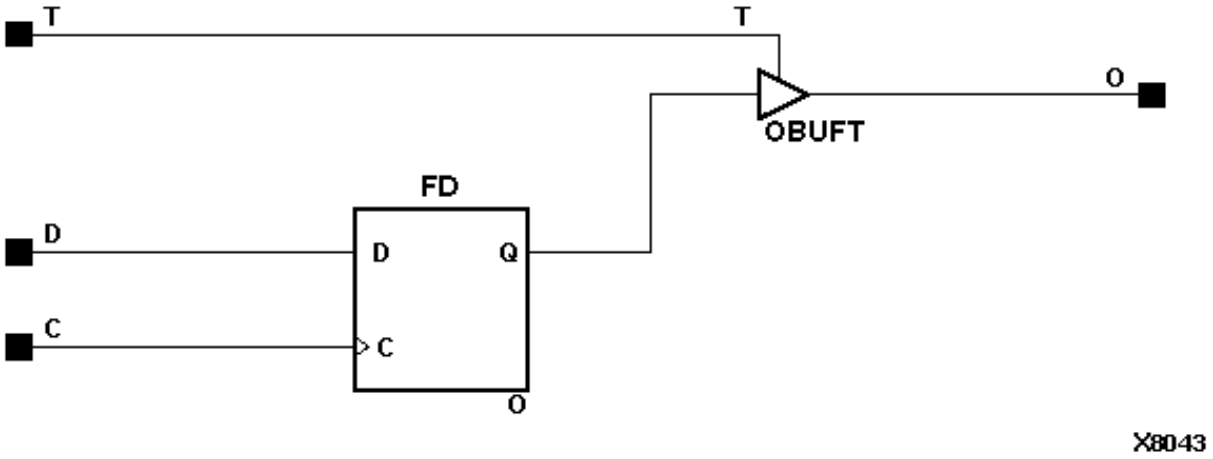
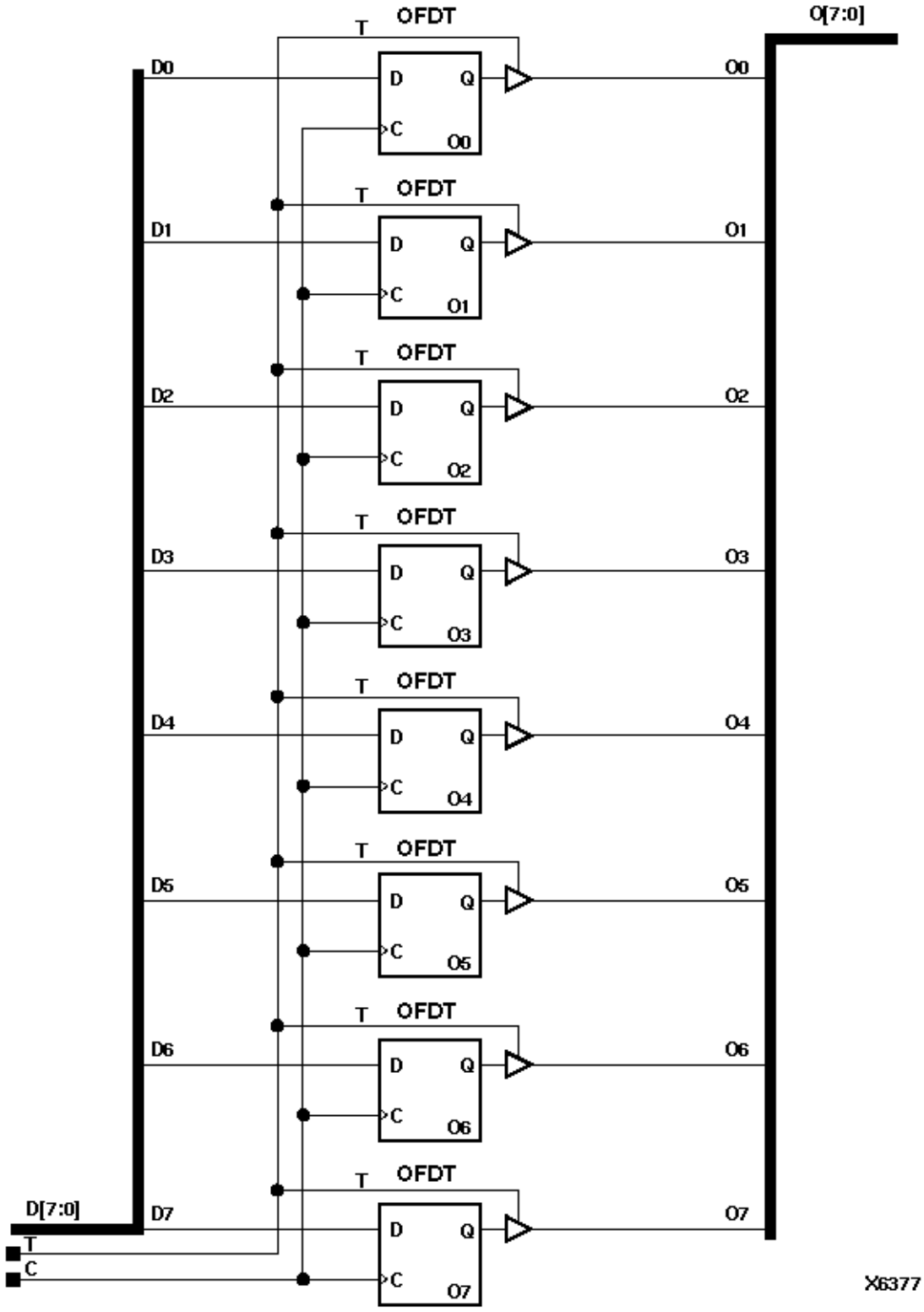


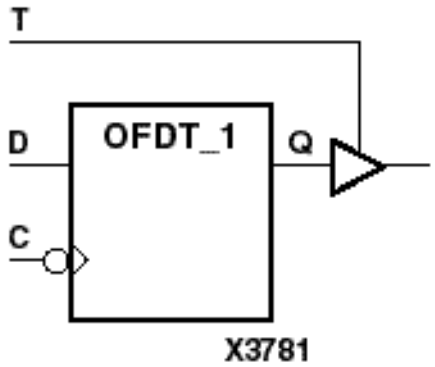
Figure 8-32OFDT8 Implementation XC3000, XC4000, XC5200, XC9000, Spartans, Virtex


OFDT
T
D
Q
C
O
D0
D1
D2
D3
D4
D5
D6
D7
O0
O1
O2
O3
O4
O5
O6
O7
O[7:0]
D[7:0]
T
C
X6377

OFDT_1

D Flip-Flop with Active-Low 3-State Output Buffer and Inverted Clock

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	N/A	Macro	Macro	Macro



OFDT_1 and its output buffer are located in an input/output block (IOB). The flip-flop data output (Q) is connected to the input of an output buffer (OBUFT). The OBUFT output is connected to an OPAD or an IOPAD. The data on the data input (D) is loaded into the flip-flop on the High-to-Low clock (C) transition. When the active-Low enable input (T) is Low, the data on the flip-flop output (Q) appears on the O output. When T is High, the output is high impedance (Off).

The flip-flop is asynchronously cleared with Low output when power is applied. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs			Outputs
T	**D**	**C**	**O**
1	X	X	Z
0	1	↓	1
0	0	↓	0

Figure 8-33OFDT_1 Implementation XC3000, XC4000, Spartans

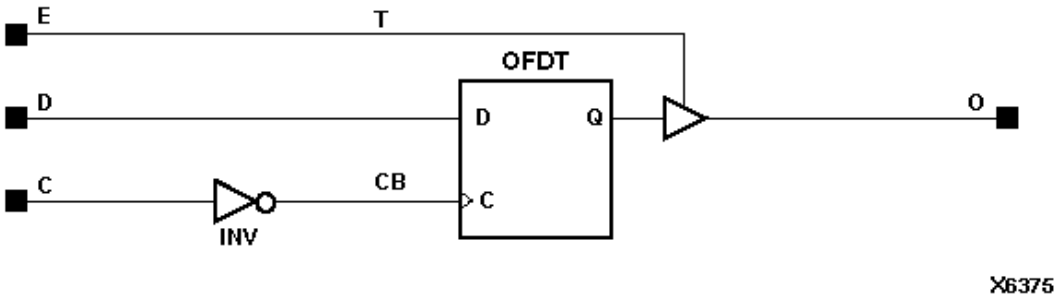
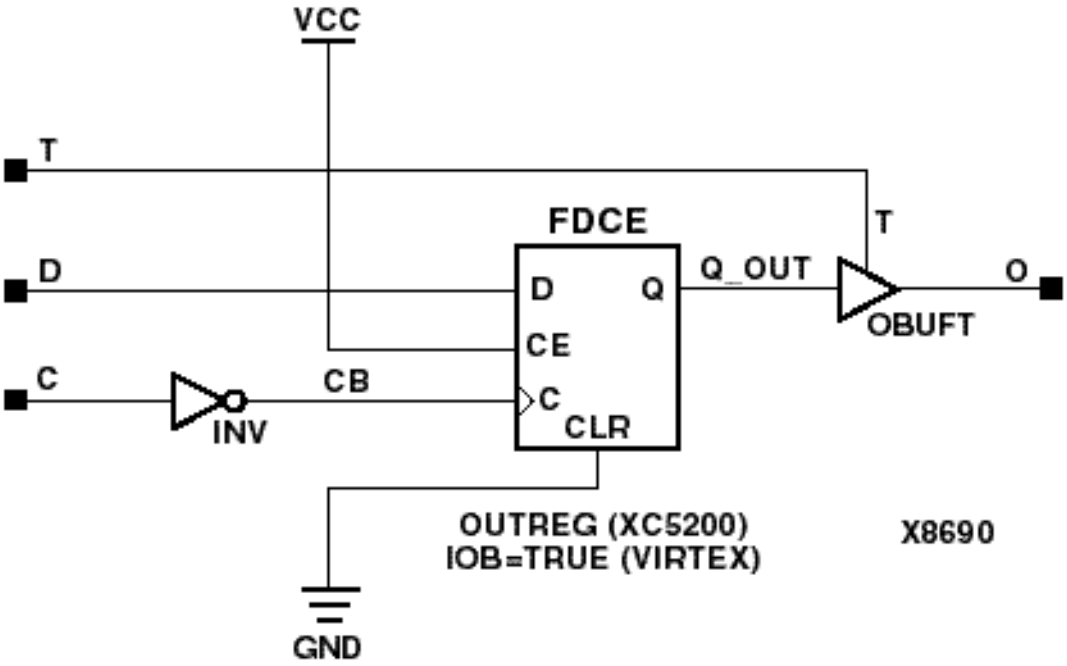


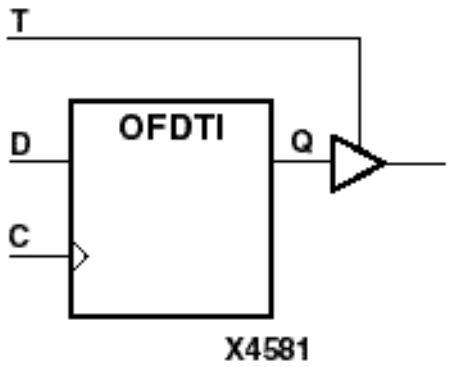
Figure 8-34OFDT_1 Implementation XC5200, Virtex



OFDTI

D Flip-Flop with Active-Low 3-State Output Buffer (Asynchronous Preset)

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	N/A	N/A	Macro	Macro	N/A

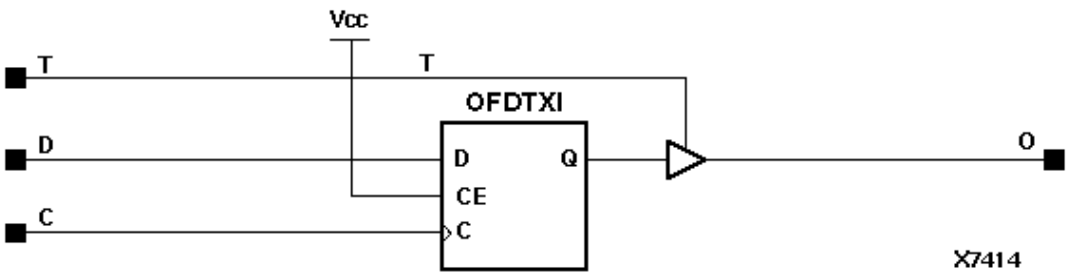


OFDTI and its output buffer are contained in an input/output block (IOB). The data output of the flip-flop (Q) is connected to the input of an output buffer (OBUFT). The output of the OBUFT is connected to an OPAD or an IOPAD. The data on the data input (D) is loaded into the flip-flop on the Low-to-High clock (C) transition. When the active-Low enable input (T) is Low, the data on the flip-flop output (Q) appears on the output (O). When T is High, the output is high impedance (off).

The flip-flop is asynchronously preset, output High, when power is applied. FPGAs simulate power-on when global set/reset (GSR) is active. GSR (XC4000, Spartans) default to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP symbol.

Inputs			Outputs
T	**D**	**C**	**O**
1	X	X	Z
0	1	↑	1
0	0	↑	0

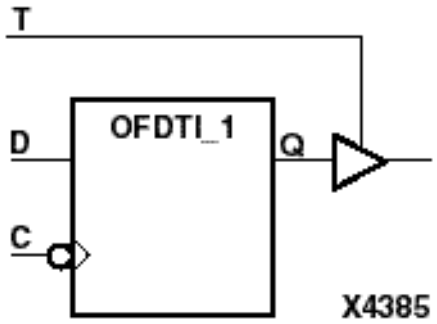
Figure 8-35OFDTI Implementation XC4000, Spartans



OFDTI_1

D Flip-Flop with Active-Low 3-State Output Buffer and Inverted Clock (Asynchronous Preset)

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	N/A	N/A	Macro	Macro	N/A

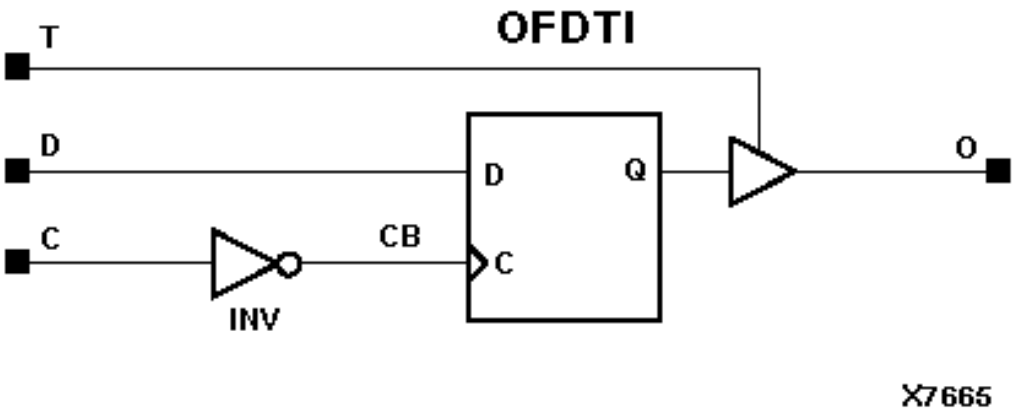


OFDTI_1 and its output buffer are contained in an input/output block (IOB). The data output of the flip-flop (Q) is connected to the input of an output buffer (OBUFT). The OBUFT output is connected to an OPAD or an IOPAD. The data on the data input (D) is loaded into the flip-flop on the High-to-Low clock (C) transition. When the active-Low enable input (T) is Low, the data on the flip-flop output (Q) appears on the O output. When T is High, the output is high impedance (off).

The flip-flop is asynchronously preset, output High, when power is applied. FPGAs simulate power-on when global set/reset (GSR) is active. GSR (XC4000, Spartans) default to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP symbol.

Inputs			Outputs
T	**D**	**C**	**O**
1	X	X	Z
0	1	↓	1
0	0	↓	0

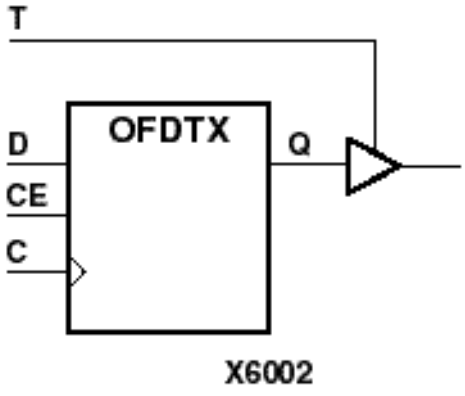
Figure 8-36OFDTI_1 Implementation XC4000, Spartans

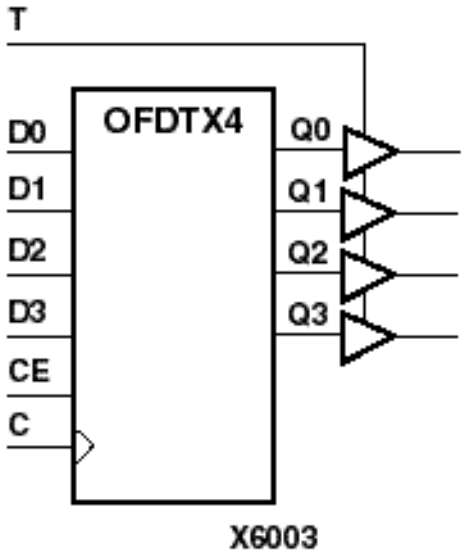


OFDTX, 4, 8, 16

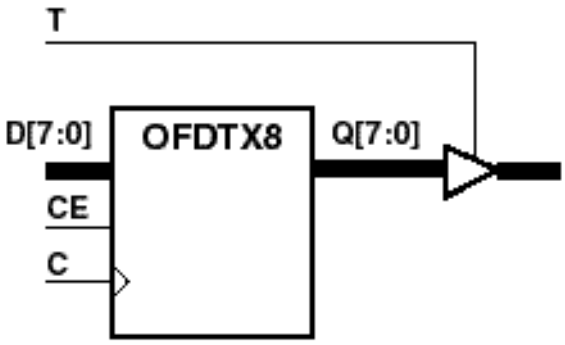
Single and Multiple D Flip-Flops with Active-Low 3-State Output Buffers and Clock Enable

Element	XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	Spartan XL	Virtex
OFDTX	N/A	Primitive	Primitive	N/A	N/A	Primitive	Primitive	N/A
OFDTX4, OFDTX8, OFDTX16	N/A	Macro	Macro	N/A	N/A	Macro	Macro	N/A

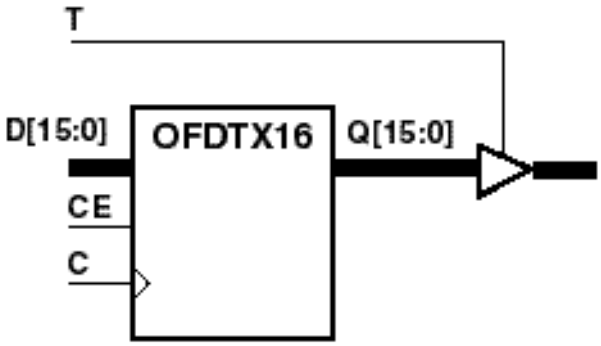




X6003



X6004



X6005

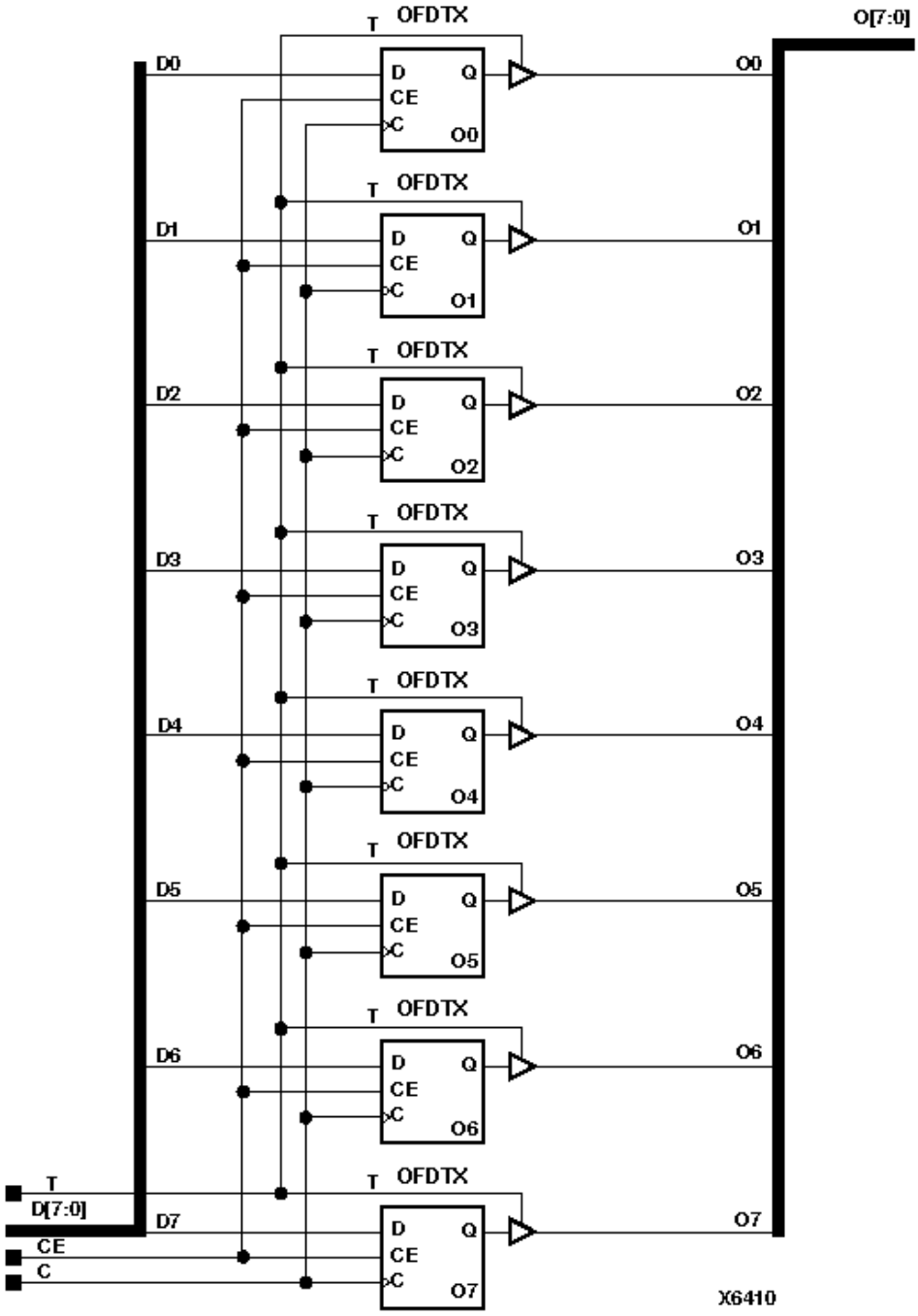
OFDTX, OFDTX4, OFDTX8, and OFDTX16 are single or multiple D flip-flops whose outputs are enabled by a tristate buffers. The data outputs (Q) of the flip-flops are connected to the inputs of output buffers (OBUFT). The outputs of the OBUFTs (O) are connected to OPADs or IOPADs. These flip-flops and buffers are located in input/output blocks (IOB) for XC4000E. The data on the data inputs (D) is loaded into the flip-flops during the Low-to-High clock (C) transition. When the active-Low enable inputs (T) are Low, the data on the flip-flop outputs (Q) appears on the O outputs. When T is High, outputs are high impedance (Off). When CE is Low and T is Low, the outputs do not change.

The flip-flops are asynchronously cleared with Low output when power is applied. FPGAs simulate power-on when global set/reset (GSR) is active. GSR (XC4000, Spartans) default to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP symbol.

Inputs				Outputs
CE	**T**	**D**	**C**	**Q**
X	1	X	X	Z
1	0	D	↑	d
0	0	X	X	No Chg

d = state of referenced input one setup time prior to active clock transition

Figure 8-37OFDTX8 Implementation XC4000, Spartans

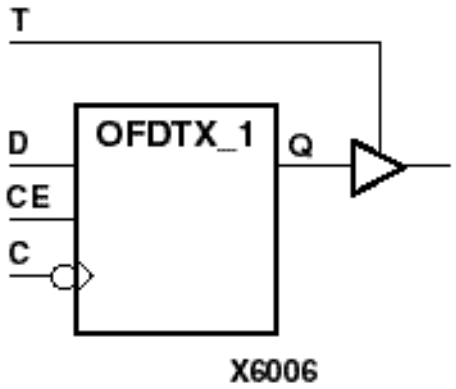


OFDTX_1

D Flip-Flop with Active-Low 3-State Output Buffer, Inverted Clock, and

Clock Enable

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	N/A	N/A	Macro	Macro	N/A

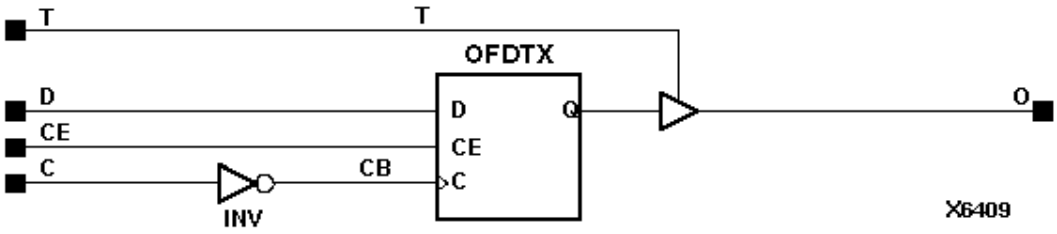


OFDTX_1 and its output buffer are located in an input/output block (IOB). The flip-flop data output (Q) is connected to the input of an output buffer (OBUFT). The OBUFT output is connected to an OPAD or an IOPAD. The data on the data input (D) is loaded into the flip-flop on the High-to-Low clock (C) transition. When the active-Low enable input (T) is Low, the data on the flip-flop output (Q) appears on the O output. When T is High, the output is high impedance (Off). When CE is High and T is Low, the outputs do not change.

The flip-flop is asynchronously cleared with Low output when power is applied. FPGAs simulate power-on when global set/reset (GSR) is active. GSR (XC4000, Spartans) default to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP symbol.

Inputs				Outputs
CE	**T**	**D**	**C**	**Q**
X	1	X	X	Z
1	0	1	↓	0
1	0	0	↓	0
0	0	X	X	No Chg

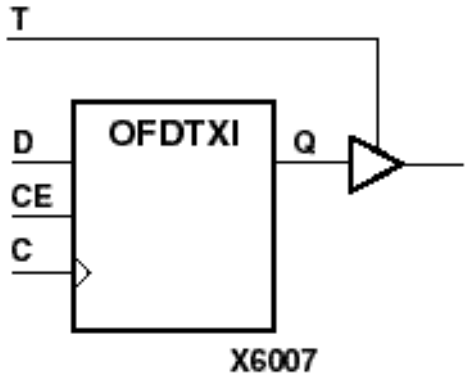
Figure 8-38OFDTX_1 Implementation XC4000, Spartans



OFDTXI

D Flip-Flop with Active-Low 3-State Output Buffer and Clock Enable (Asynchronous Preset)

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Primitive	Primitive	N/A	N/A	Primitive	Primitive	N/A



OFDTXI and its output buffer are contained in an input/output block (IOB). The data output of the flip-flop (Q) is connected to the input of an output buffer (OBUFT). The output of the OBUFT is connected to an OPAD or an IOPAD. The data on the data input (D) is loaded into the flip-flop on the Low-to-High clock (C) transition. When the active-Low enable input (T) is Low, the data on the flip-flop output (Q) appears on the output (O). When T is High, the output is high impedance (Off). When CE is Low and T is Low, the output does not change.

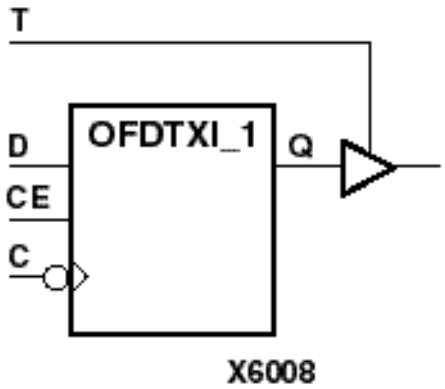
The flip-flop is asynchronously preset with High output when power is applied. FPGAs simulate power-on when global set/reset (GSR) is active. GSR (XC4000, Spartans) default to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP symbol.

Inputs				Outputs
CE	**T**	**D**	**C**	**O**
X	1	X	X	Z
1	0	1	↑	1
1	0	0	↑	0
0	0	X	X	No Chg

OFDTXI_1

D Flip-Flop with Active-Low 3-State Output Buffer, Inverted Clock, and Clock Enable (Asynchronous Preset)

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	N/A	N/A	Macro	Macro	N/A

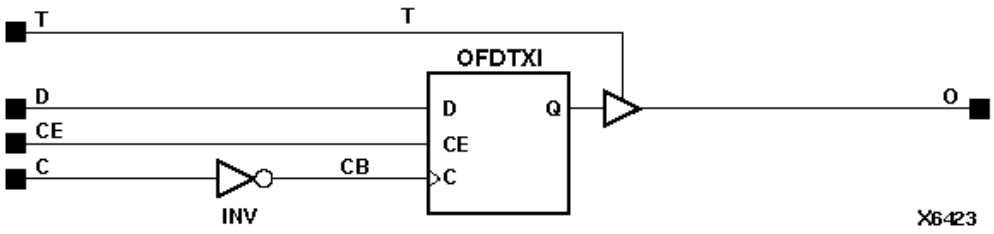


OFDTXI_1 and its output buffer are contained in an input/output block (IOB). The data output of the flip-flop (Q) is connected to the input of an output buffer (OBUFT). The OBUFT output is connected to an OPAD or an IOPAD. The data on the data input (D) is loaded into the flip-flop on the High-to-Low clock (C) transition. When the active-Low enable input (T) is Low, the data on the flip-flop output (Q) appears on the O output. When T is High, the output is high impedance (Off). When CE is Low and T is Low, the output does not change.

The flip-flop is asynchronously preset with High output when power is applied. FPGAs simulate power-on when global set/reset (GSR) is active. GSR (XC4000, Spartans) default to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP symbol.

Inputs				Outputs
CE	**T**	**D**	**C**	**Q**
X	1	X	X	Z
1	0	1	↓	1
1	0	0	↓	0
0	0	X	X	No Chg

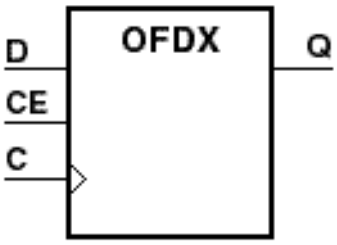
Figure 8-39OFDTXI_1 Implementation XC4000, Spartans



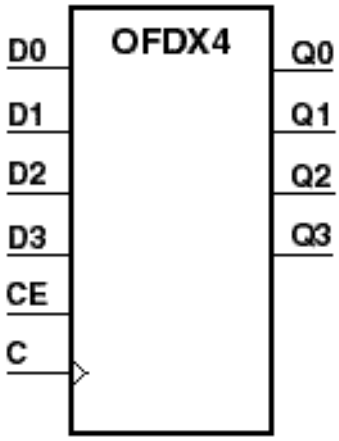
OFDX, 4, 8, 16

Single- and Multiple-Output D Flip-Flops with Clock Enable

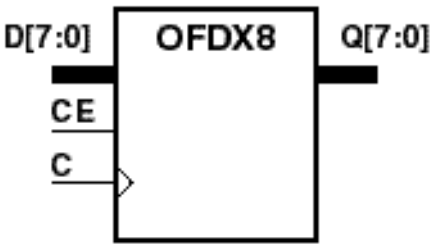
Element	XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	Spartan XL	Virtex
OFDX	N/A	Primitive	Primitive	N/A	N/A	Primitive	Primitive	Macro
OFDX4, OFDX8, OFDX16	N/A	Macro	Macro	N/A	N/A	Macro	Macro	Macro



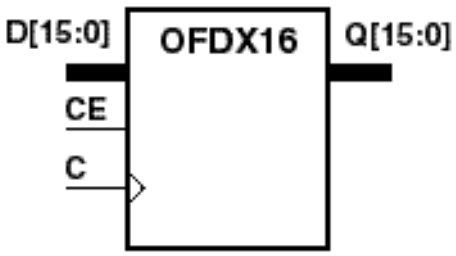
X4988



X4989



X4990



X4991

OFDX, OFDX4, OFDX8, and OFDX16 are single and multiple output D flip-flops. The flip-flops are located in an input/output block (IOB) for XC4000E. The Q outputs are connected to OPADs or IOPADs. The data on the D inputs is loaded into the flip-flops during the Low-to-High clock (C) transition and appears on the Q outputs. When CE is Low, flip-flop outputs do not change.

The flip-flops are asynchronously cleared with Low outputs, when power is applied. FPGAs simulate power-on when

global set/reset (GSR) is active. GSR (XC4000, Spartans) default to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP symbol.

Inputs			Outputs
CE	**D**	**C**	**Q**
1	D	↑	dn
0	X	X	No Chg

dn = state of referenced input one setup time prior to active clock transition

Figure 8-40OFDX Implementation Virtex

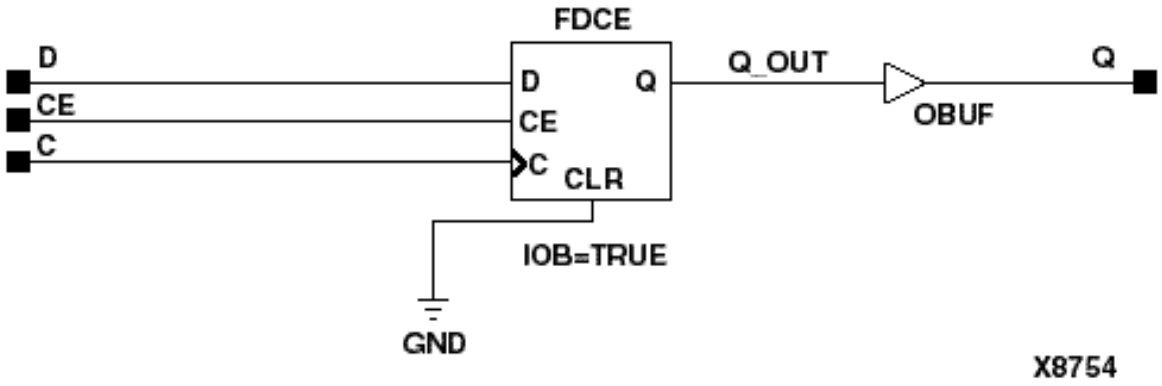
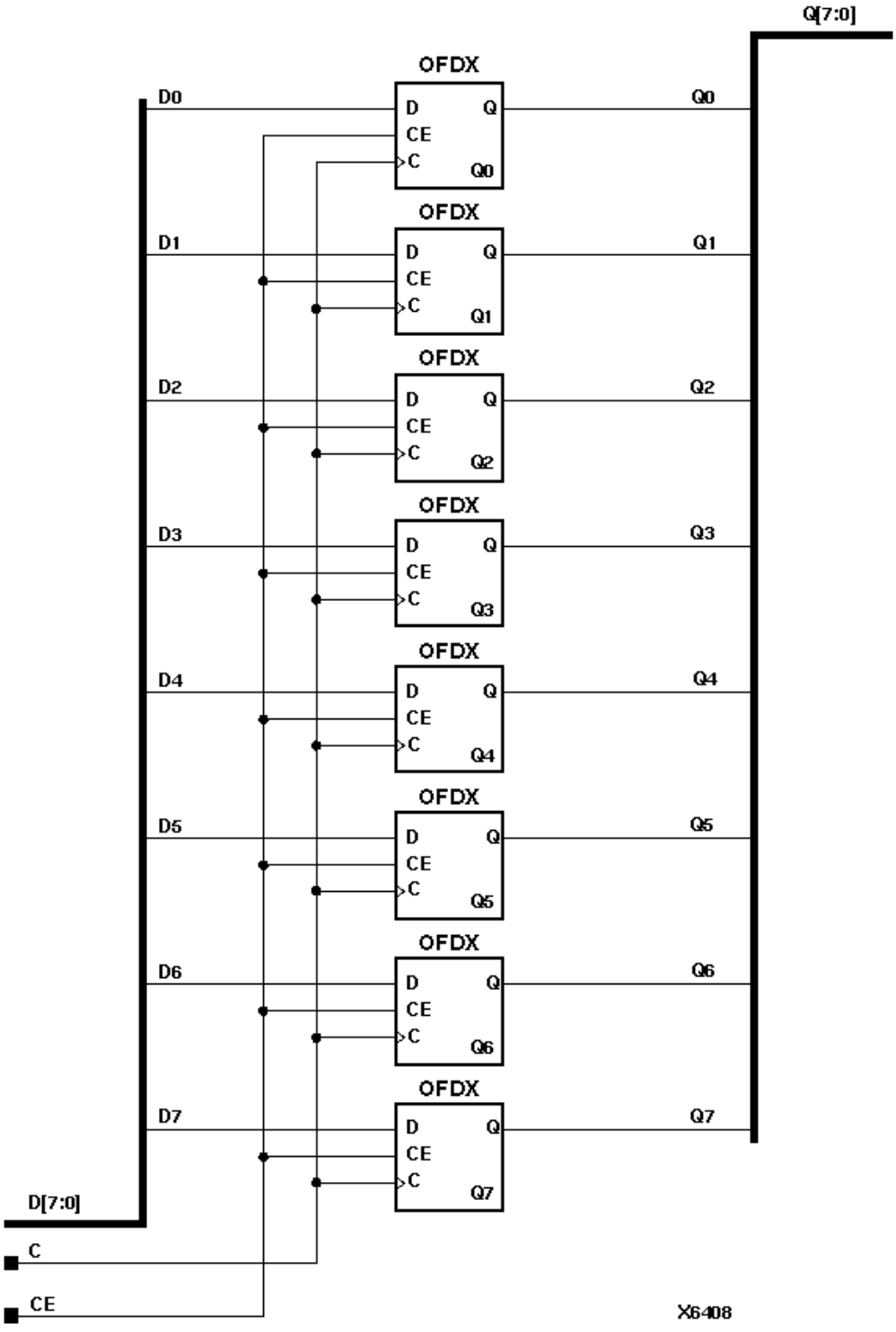


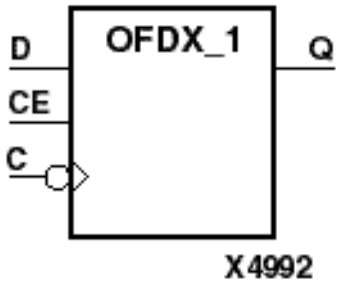
Figure 8-41OFDX8 Implementation XC4000, Spartans, Virtex


Q[7:0]
OFDX
D0
D
CE
C
Q
Q0
Q0
D1
Q1
Q1
D2
Q2
Q2
D3
Q3
Q3
D4
Q4
Q4
D5
Q5
Q5
D6
Q6
Q6
D7
Q7
Q7
D[7:0]
C
CE
X6408

OFDX_1

Output D Flip-Flop with Inverted Clock and Clock Enable

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	N/A	N/A	Macro	Macro	Macro



OFDX_1 is located in an input/output block (IOB). The output (Q) of the D flip-flop is connected to an OPAD or an IOPAD. The data on the D input is loaded into the flip-flop during the High-to-Low clock (C) transition and appears on the Q output. When the CE pin is Low, the output (Q) does not change.

The flip-flop is asynchronously cleared with Low output when power is applied. FPGAs simulate power-on when global set/reset (GSR) is active. GSR (XC4000, Spartans) default to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP symbol.

Inputs			Outputs
CE	**D**	**C**	**Q**
1	D	↓	d
0	X	X	No Chg

d = state of referenced input one setup time prior to active clock transition

Figure 8-42OFDX_1 Implementation XC4000, Spartans

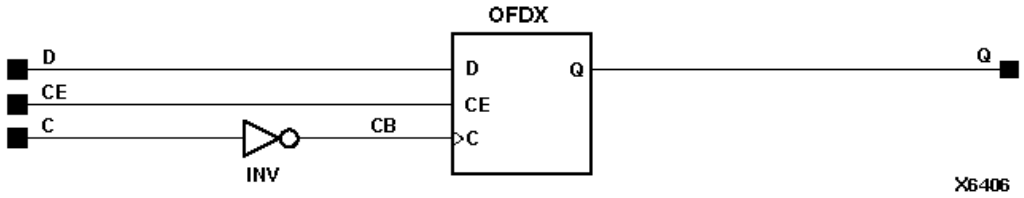
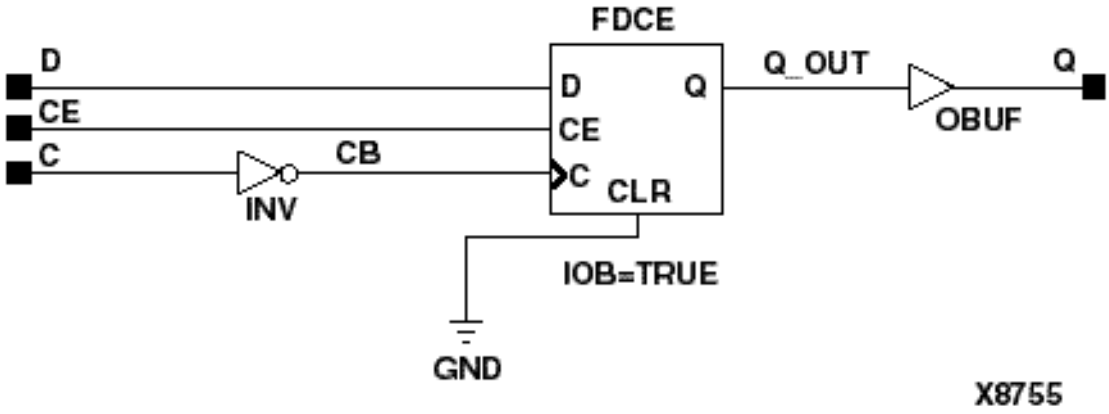


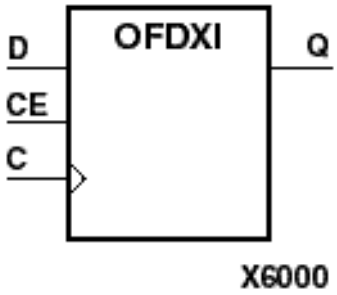
Figure 8-43OFDX_1 Implementation Virtex



OFDXI

Output D Flip-Flop with Clock Enable (Asynchronous Preset)

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Primitive	Primitive	N/A	N/A	Primitive	Primitive	Macro



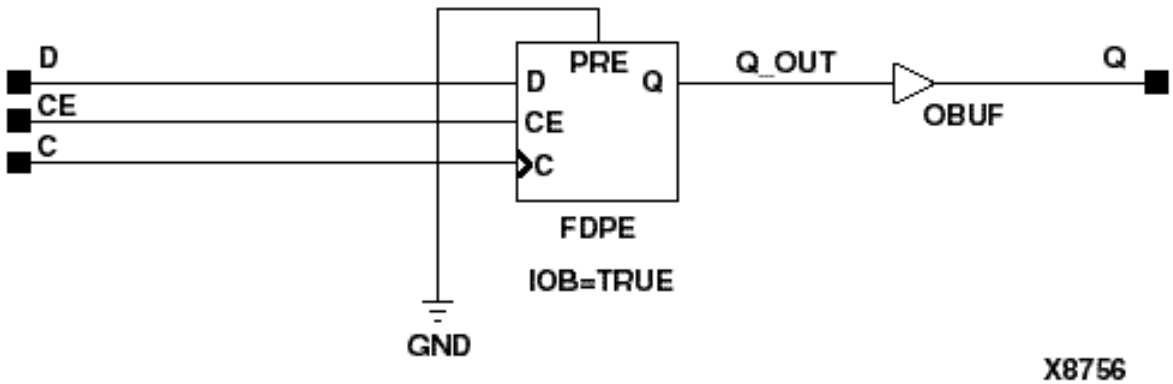
OFDXI is contained in an input/output block (IOB). The output (Q) of the D flip-flop is connected to an OPAD or an IOPAD. The data on the D input is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). When CE is Low, the output does not change.

The flip-flop is asynchronously preset with High output when power is applied. FPGAs simulate power-on when global set/reset (GSR) is active. GSR (XC4000, Spartans) default to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP symbol.

Inputs			Outputs
CE	**D**	**C**	**Q**
1	D	↑	d
0	X	X	No Chg

d = state of referenced input one setup time prior to active clock transition

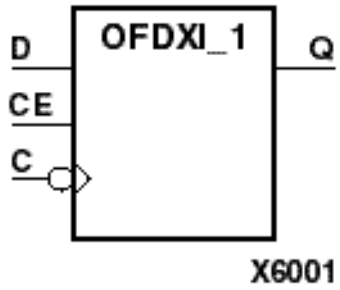
Figure 8-44OFDXI Implementation Virtex



OFDXI_1

Output D Flip-Flop with Inverted Clock and Clock Enable (Asynchronous Preset)

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	N/A	N/A	Macro	Macro	Macro



OFDXI_1 is located in an input/output block (IOB). The D flip-flop output (Q) is connected to an OPAD or an IOPAD. The data on the D input is loaded into the flip-flop during the High-to-Low clock (C) transition and appears on the Q output. When CE is Low, the output (Q) does not change.

The flip-flop is asynchronously preset with High output when power is applied. FPGAs simulate power-on when global set/reset (GSR) is active. GSR (XC4000, Spartans) default to active-High but can be inverted by adding an inverter in front of the GSR input of the STARTUP symbol.

Inputs			Outputs
CE	**D**	**C**	**Q**
1	D	↓	d
0	X	X	No Chg

d = state of referenced input one setup time prior to active clock transition

Figure 8-45OFDXI_1 Implementation XC4000, Spartans

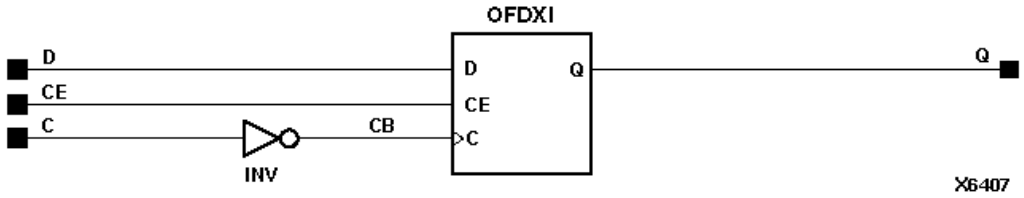
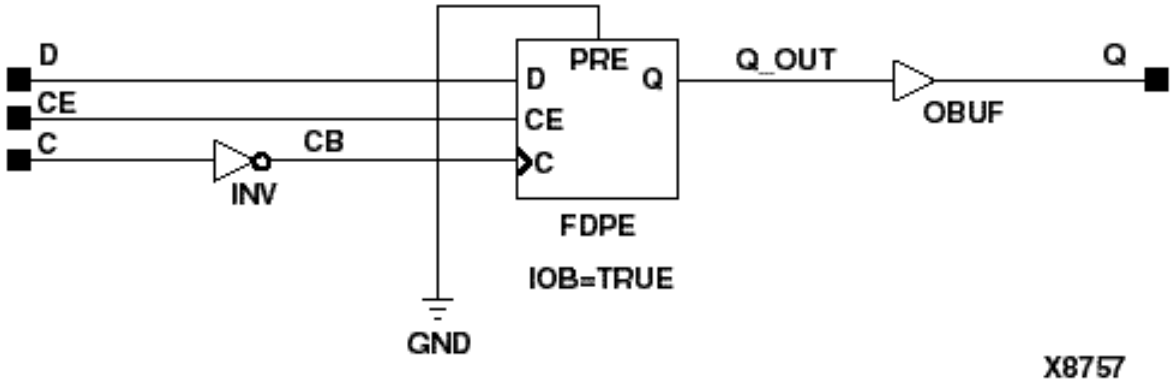


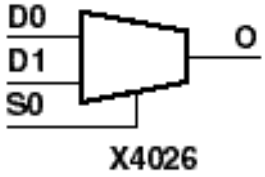
Figure 8-46OFDXI_1 Implementation Virtex



OMUX2

2-to-1 Multiplexer

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	Primitive	N/A	N/A	N/A	Primitive	N/A



The OMUX2 multiplexer chooses one data bit from two sources (D1 or D0) under the control of the select input (S0). The output (O) reflects the state of the selected data input. When Low, S0 selects D0 and when High, S0 selects

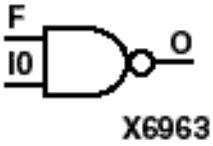
D1.

Inputs			Outputs
S0	**D1**	**D0**	**O**
1	1	X	1
1	0	X	0
0	X	1	1
0	X	0	0

ONAND2

2-Input NAND Gate with Invertible Inputs

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	Primitive	N/A	N/A	N/A	Primitive	N/A

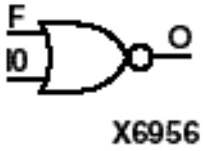


ONAND2 is a 2-input NAND gate that is implemented in the output multiplexer of the XC4000X IOB. The F pin is faster than I0. Input pins can be inverted even though there is no library component showing inverted inputs. The mapper will automatically bring any inverted input pins into the IOB.

ONOR2

2-Input NOR Gate with Invertible Inputs

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	Primitive	N/A	N/A	N/A	Primitive	N/A

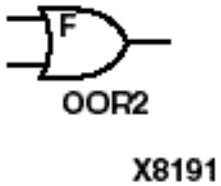


ONOR2 is a 2-input NOR gate that is implemented in the output multiplexer of the XC4000X IOB. The F pin is faster than I0. Input pins can be inverted even though there is no library component showing inverted inputs. The mapper will automatically bring any inverted input pins into the IOB.

OOR2

2-Input OR Gate with Invertible Inputs

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	Primitive	N/A	N/A	N/A	Primitive	N/A

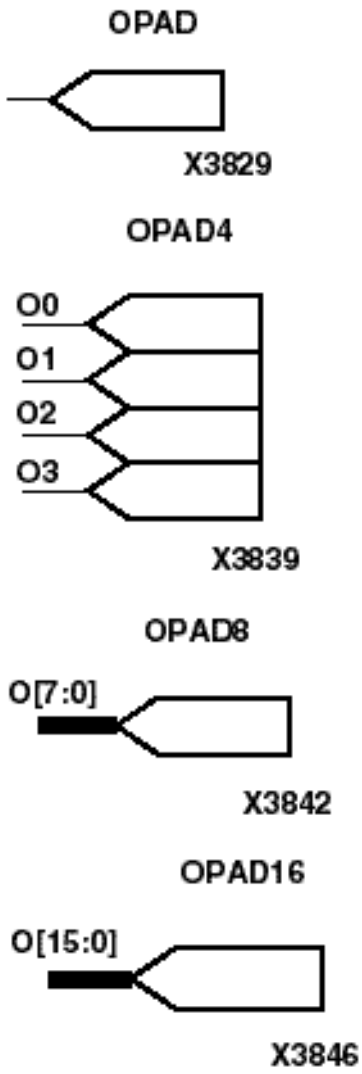


OOR2 is a 2-input OR gate that is implemented in the output multiplexer of the XC4000X IOB. The F pin is faster than I0. Input pins can be inverted even though there is no library component showing inverted inputs. The mapper will automatically bring any inverted input pins into the IOB.

OPAD, 4, 8, 16

Single- and Multiple-Output Pads

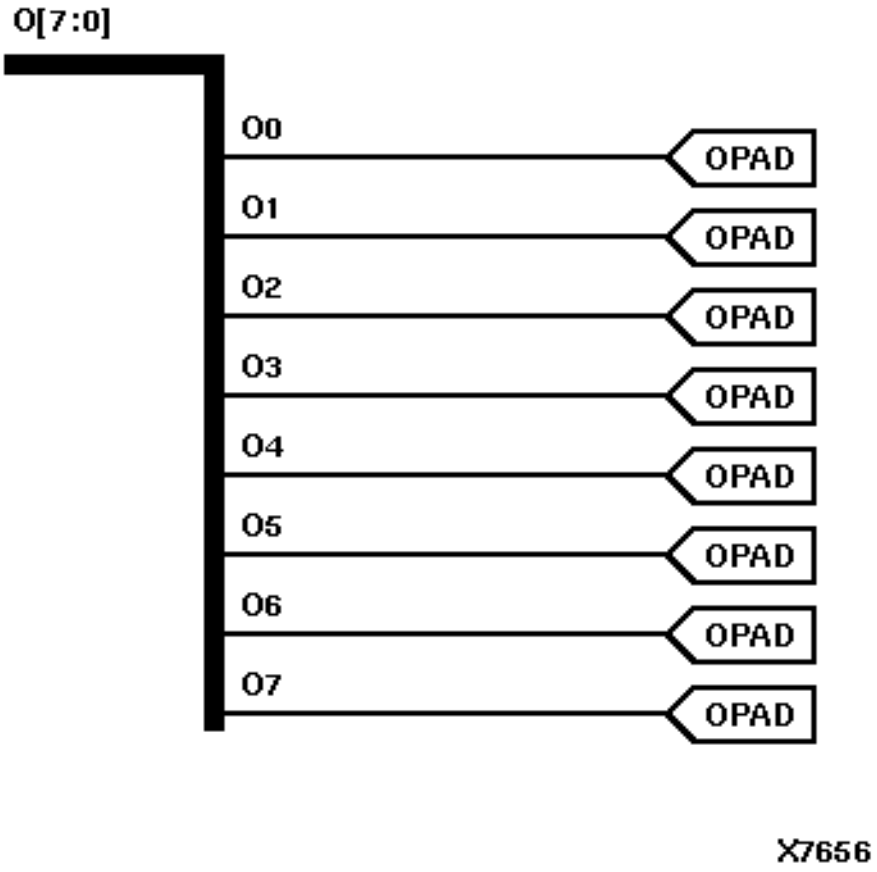
Element	XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	Spartan XL	Virtex
OPAD	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
OPAD4, OPAD8, OPAD16	Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro



OPAD, OPAD4, OPAD8, and OPAD16 are single and multiple output pads. An OPAD connects a device pin to an output signal of a PLD. It is internally connected to an input/output block (IOB), which is configured by the software as an OBUF, an OBUFT, an OBUFE, an OFD, or an OFDT.

Refer to the appropriate CAE tool interface user guide for details on assigning pin location and identification.

Figure 8-47OPAD8 Implementation XC3000, XC4000, XC5200, XC9000, Spartans, Virtex



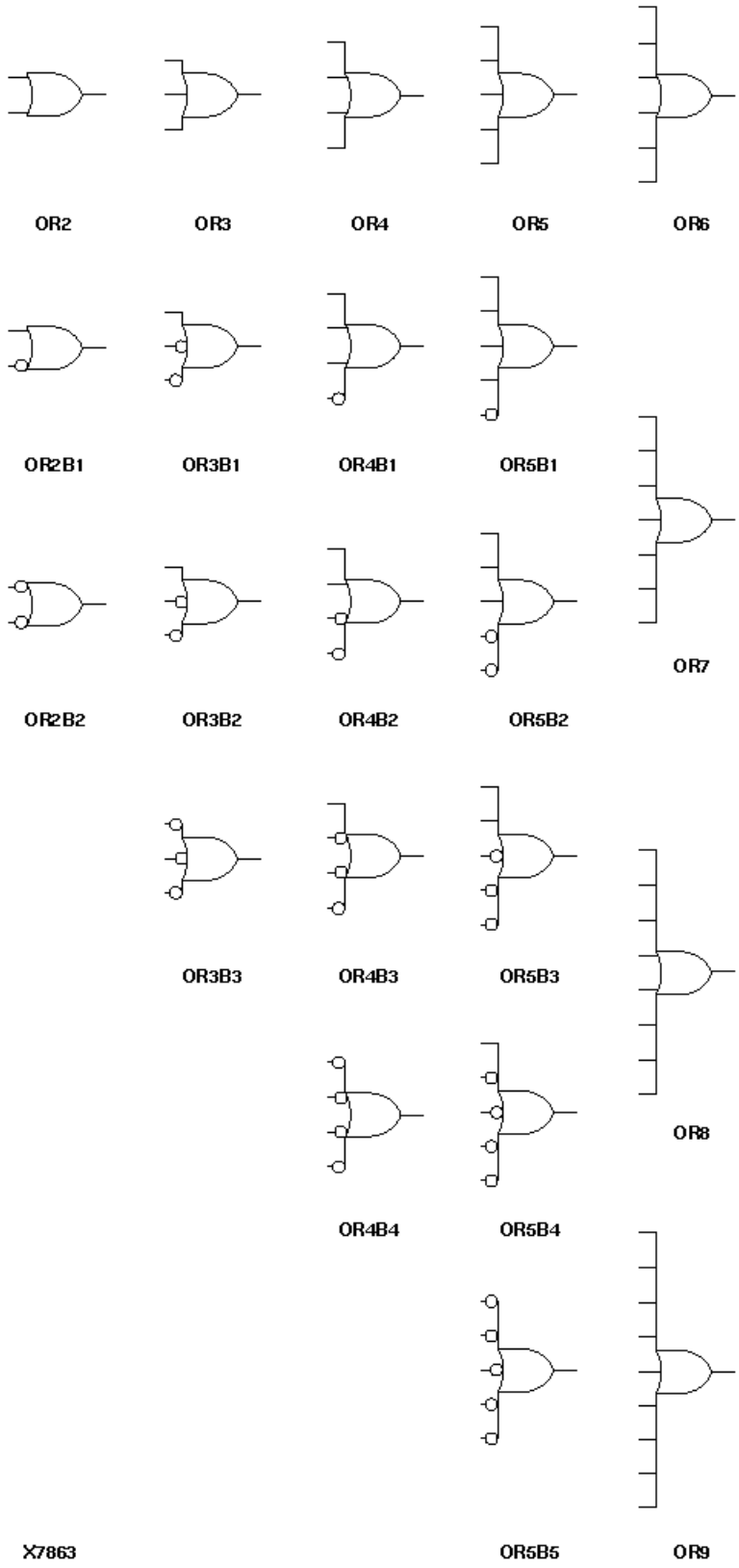
OR2-9

2- to 9-Input OR Gates with Inverted and Non-Inverted Inputs

Element	XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	Spartan XL	Virtex
OR2, OR2B1, OR2B2, OR3, OR3B1, OR3B2,	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive

OR3B3, OR4, OR4B1, OR4B2, OR4B3, OR4B4								
OR5, OR5B1, OR5B2, OR5B3, OR5B4, OR5B5	Primitive	Primitive	Primitive	Macro	Primitive	Primitive	Primitive	Primitive
OR6, OR7, OR8, OR9	Macro	Macro	Macro	Macro	Primitive	Macro	Macro	Macro

Figure 8-48OR Gate Representations


OR2
OR3
OR4
OR5
OR6
OR2B1
OR3B1
OR4B1
OR5B1
OR7
OR2B2
OR3B2
OR4B2
OR5B2
OR3B3
OR4B3
OR5B3
OR8
OR4B4
OR5B4
OR5B5
OR9
X7863

The OR function is performed in the Configurable Logic Block (CLB) function generators for FPGAs. OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Since each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Refer to the **"OR12, 16"** section for information on additional OR functions for the XC5200 and Virtex.

Figure 8-49OR5 Implementation XC5200

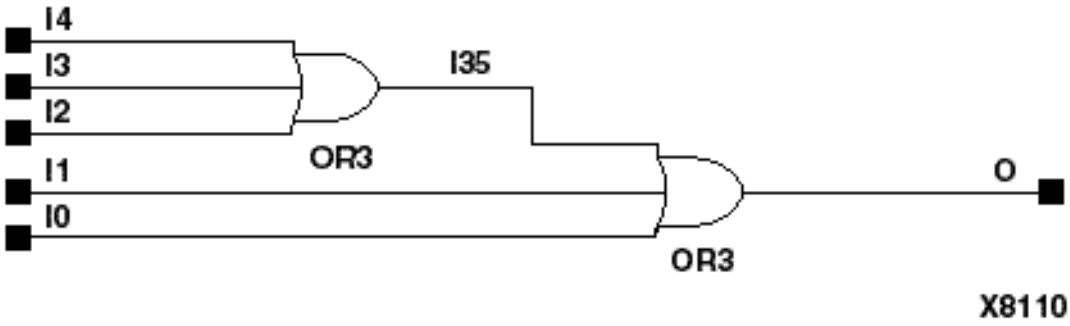


Figure 8-50OR8 Implementation XC3000

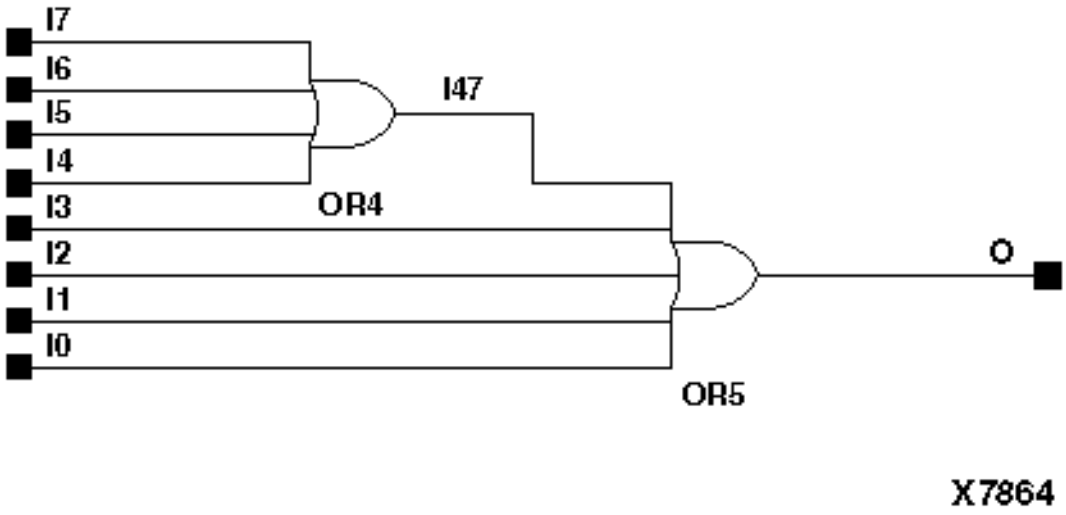


Figure 8-51OR8 Implementation XC4000, XC5200, Spartans

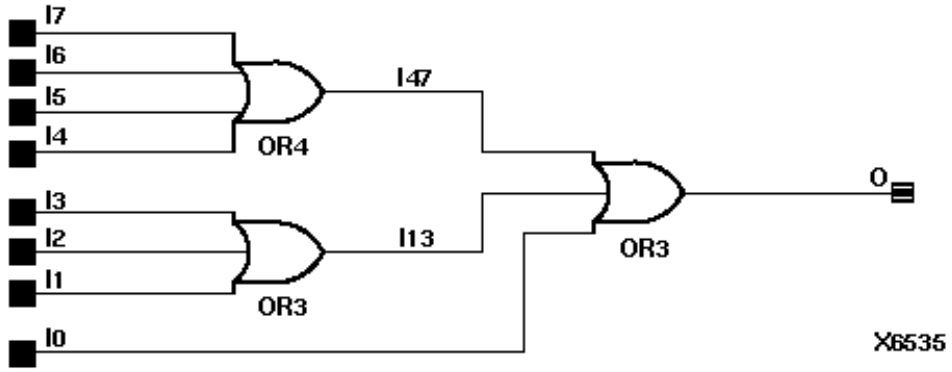
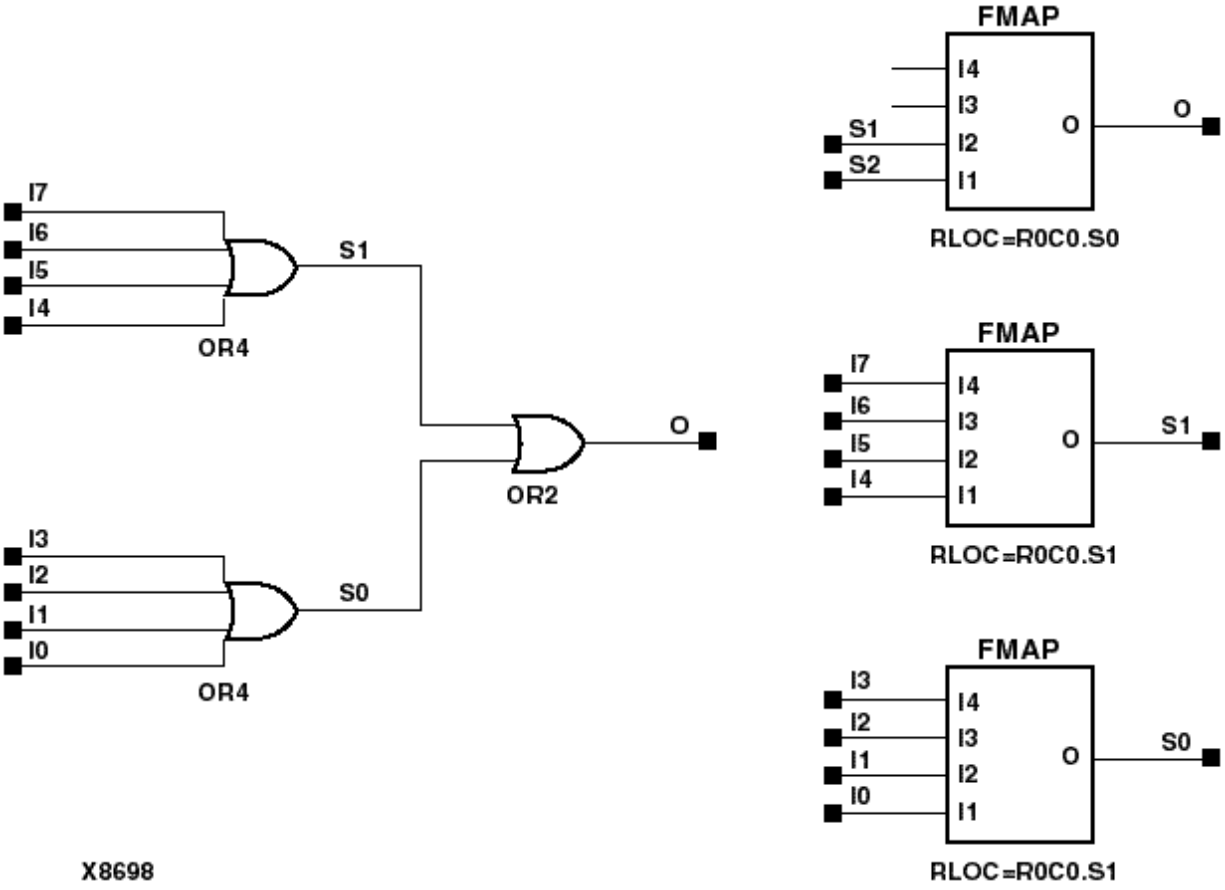


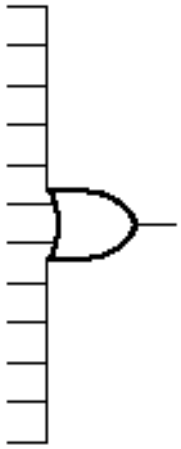
Figure 8-52OR8 Implementation Virtex



OR12, 16

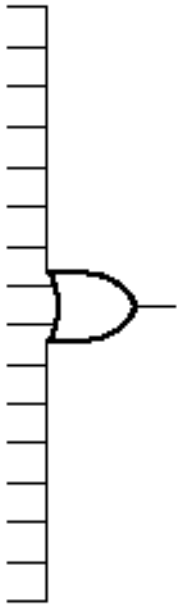
12- and 16-Input OR Gates with Non-Inverted Inputs

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	N/A	Macro	N/A	N/A	N/A	Macro



OR12

X8198



OR16

X8199

Refer to the **"OR2-9"** section for information on OR functions.

Figure 8-53OR16 Implementation XC5200

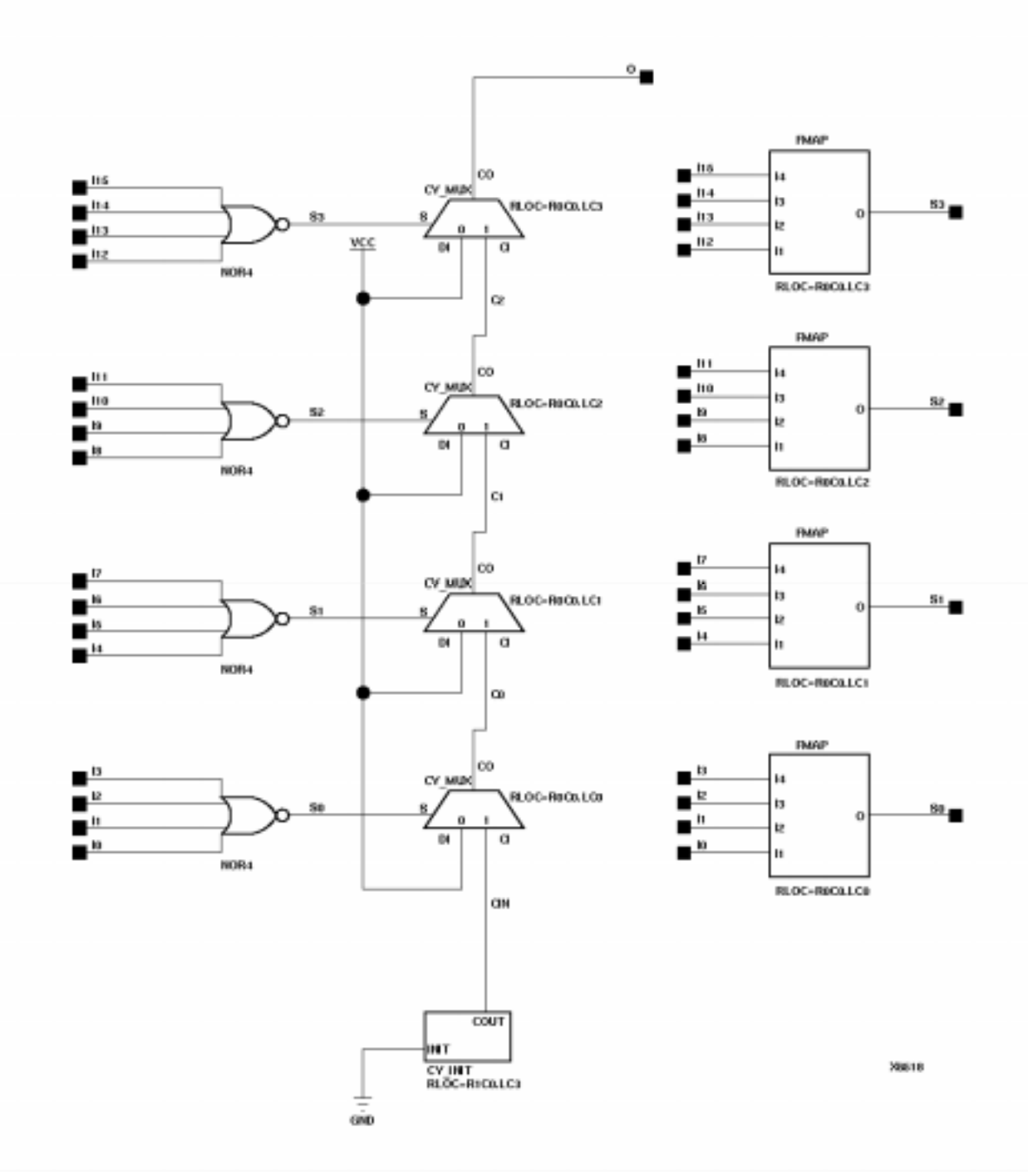
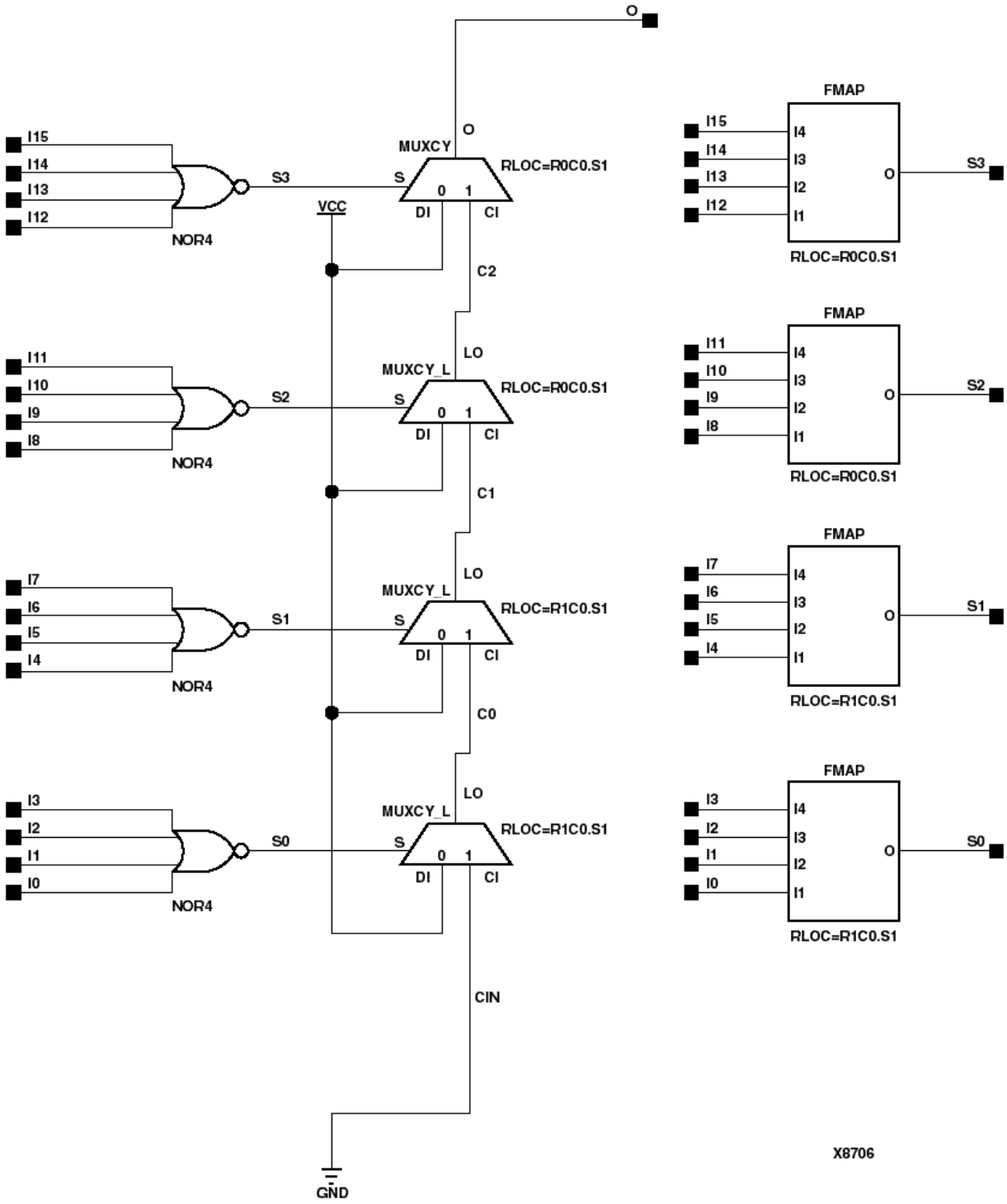


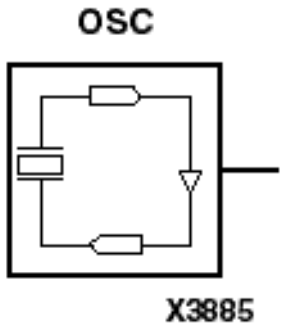
Figure 8-54OR16 Implementation Virtex



OSC

Crystal Oscillator Amplifier

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Primitive	N/A	N/A	N/A	N/A	N/A	N/A	N/A



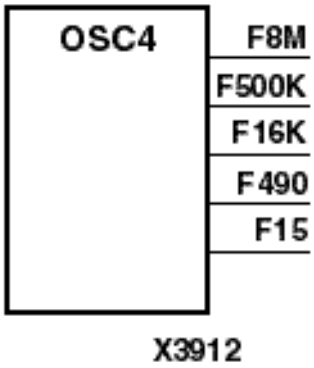
The OSC element's clock signal frequency is derived from an external crystal-controlled oscillator. The OSC output can be connected to an ACLK buffer, which is connected to an internal clock net.

Two dedicated input pins (XTAL 1 and XTAL 2) on each FPGA device are internally connected to pads and input/output blocks that are connected to the OSC amplifier. The external components are connected as shown in the following example. Refer to *The Programmable Logic Data Book* for details on component selection and tolerances.

OSC4

Internal 5-Frequency Clock-Signal Generator

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Primitive	Primitive	N/A	N/A	Primitive	Primitive	N/A



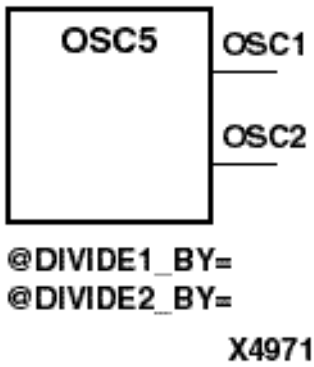
OSC4 provides internal clock signals in applications where timing is not critical. The available frequencies are determined by FPGA device components, which are process dependent. Therefore, the available frequencies vary from device to device. Nominal frequencies are 8 MHz, 500 kHz, 16 kHz, 490 Hz, and 15 Hz. Although there are five

outputs, only three can be used at a time, with 8 MHz on one output and one frequency each on any two of the remaining four outputs. An error occurs if more than three outputs are used simultaneously.

OSC5

Internal Multiple-Frequency Clock-Signal Generator

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	N/A	Primitive	N/A	N/A	N/A	N/A



OSC5 provides internal clock signals in applications where timing is not critical. The available frequencies are determined by FPGA device components that are process dependent. Therefore, the available frequencies vary from device to device. Use only one OSC5 per design. The OSC5 is not available if the CK_DIV element is used.

The clock frequencies of the OSC1 and OSC2 outputs are determined by specifying the DIVIDE1_BY=n_1 attribute for the OSC1 output and the DIVIDE2_BY=n_2 attribute for the OSC2 output. n_1 and n_2 are integer numbers by which the internal 16-MHz clock is divided to produce the desired clock frequency. The available frequency options are shown in the table.

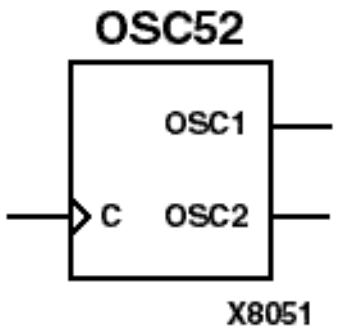
n_1	OSC1 Frequency	n_2	OSC2 Frequency
4	4 MHz	2	8 MHz
16	1 MHz	8	2 MHz
64	250 kHz	32	500 kHz
256	63 kHz	128	125 kHz
		1,024	16 kHz

	4,096	4 kHz
	16,384	1 kHz
	65,536	244 Hz

OSC52

Internal Multiple-Frequency Clock-Signal Generator

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	N/A	Primitive	N/A	N/A	N/A	N/A



OSC52 provides internal clock signals in applications where timing is not critical. The available frequencies are determined by FPGA device components, which are process independent. Therefore, the available frequencies vary from device to device. Only one OSC52 may be used per design.

The oscillator frequencies of the OSC1 and OSC2 outputs are determined by specifying theDIVIDE1_BY=n_1 attribute for the OSC1 output and DIVIDE2_BY=n_2 attribute for the OSC2 output. n_1 and n_2 are integer numbers by which internal 16-MHz clock is divided to produce the desired clock frequency. The available frequency options appear in the table that follows.

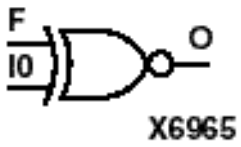
n_1	OSC1 Frequency	n_2	OSC2 Frequency
4	4 MHz	2	8 MHz
16	1 MHz	8	2 MHz
64	250 kHz	32	500 kHz
256	63 kHz	128	125 kHz
		1,024	16 kHz

	4,096	4 kHz
	16,384	1 kHz
	65,536	244 Hz

OXNOR2

2-Input Exclusive-NOR Gate with Invertible Inputs

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	Primitive	N/A	N/A	N/A	Primitive	N/A



OXNOR2 is a 2-input exclusive NOR gate that is implemented in the output multiplexer of the XC4000X and SpartanXL IOB. The F pin is faster than I0. Input pins can be inverted even though there is no library component showing inverted inputs. The mapper will automatically bring any inverted input pins into the IOB.

OXOR2

2-Input Exclusive-OR Gate with Invertible Inputs

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	Primitive	N/A	N/A	N/A	Primitive	N/A

X6964

OXOR2 is a 2-input exclusive OR gate that is implemented in the output multiplexer of the XC4000X IOB. The F pin is faster than I0. Input pins can be inverted even though there is no library component showing inverted inputs. The mapper will automatically bring any inverted input pins into the IOB.