Chapter 4

Design Elements (CAPTURE_VIRTEX to DECODE64)

This chapter describes design elements included in the Unified Libraries. The elements are organized in alphanumeric order with all numeric suffixes in ascending order.

Information on the specific architectures supported by each of the following libraries is contained under the Applicable Architectures section of the Unified Libraries Chapter.

- **XC3000 Library**
- **XC4000E Library**
- **XC4000X Library**
- **XC5200 Library**
- **XC9000 Library**
- **Spartan Library**
- **SpartanXL Library**
- **Virtex Library**

Note: Wherever *XC4000* is mentioned, the information applies to all architectures supported by the XC4000E and XC4000X libraries.

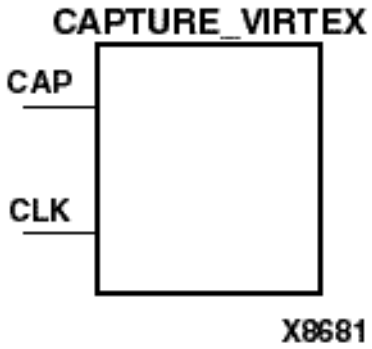
Note: Wherever *Spartans* or *Spartan series* is mentioned, the information applies to all architectures supported by the Spartan and SpartanXL libraries.

Schematics are included for each library if the implementation differs. Design elements with bused or multiple I/O pins (2-, 4-, 8-, 16-bit versions) typically include just one schematic — generally the 8-bit version. When only one schematic is included, implementation of the smaller and larger elements differs only in the number of sections. In cases where an 8-bit version is very large, an appropriate smaller element serves as the schematic example.

CAPTURE_VIRTEX

Virtex Register State Capture for Bitstream Readback

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
N/A	N/A	N/A	N/A	N/A	N/A	N/A	Primitive



CAPTURE_VIRTEX provides user control over when to capture register (flip-flop and latch) information for readback. Virtex provides the readback function through dedicated configuration port instructions, instead of with a READBACK component as in other FPGA architectures. The CAPTURE_VIRTEX symbol is optional. Without it readback is still performed, but the asynchronous capture function it provides for register states is not available.

Note: Virtex only allows for capturing register (flip-flop and latch) states. Although LUT RAM, SRL, and block RAM states are read back, they cannot be captured.

An asserted High CAP signal indicates that the registers in the device are to be captured at the next Low-to-High clock transition. The Low-to-High clock transition triggers the capture clock (CLK) which clocks out the readback data.

Two BitGen options control when capture can occur.

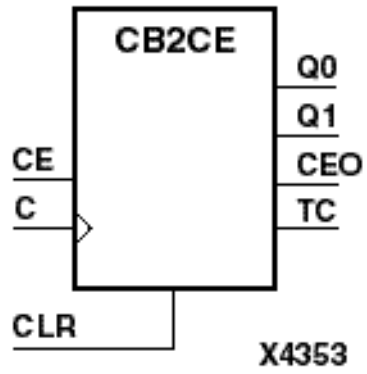
- When ONESHOT mode is set, only a single capture of registers for readback is allowed. After a trigger (transition on CLK while CAP is asserted), all register information is captured and no additional captures can occur until the readback operation is completed.
- When CONTINUOUS mode is set, data is captured after every trigger (transition on CLK while CAP is asserted).

For details on the Virtex readback function, refer to the Xilinx web site, http://www.xilinx.com.

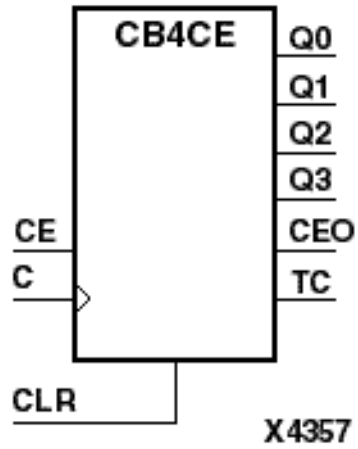
CB2CE, CB4CE, CB8CE, CB16CE

2-, 4-, 8-,16-Bit Cascadable Binary Counters with Clock Enable and Asynchronous Clear

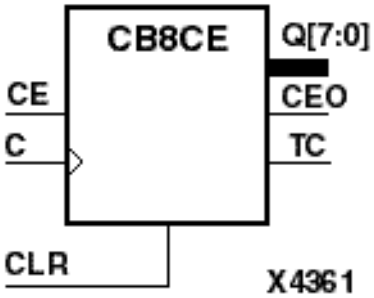
XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro



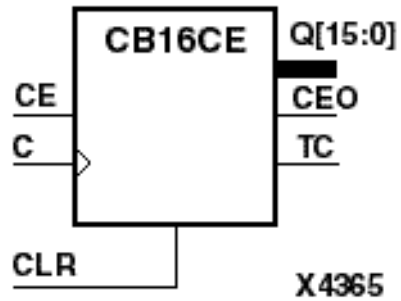
X4353



X4357



X4361



X4365

CB2CE, CB4CE, CB8CE, and CB16CE are, respectively, 2-, 4-, 8-, and 16-bit (stage), asynchronous, clearable, cascadable binary counters. The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other

inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Larger counters are created by connecting the CEO output of the first stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE\text{-}TC})$, where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input; use the TC output if it does not.

The counter is asynchronously cleared, outputs Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs			**Outputs**		
CLR	**CE**	**C**	**Qz – Q0**	**TC**	**CEO**
1	X	X	0	0	0
0	0	X	No Chg	No Chg	0
0	1	↑	Inc	TC	CEO

z= 1 for CB2CE; z = 3 for CB4CE; z = 7 for CB8CE; z = 15 for CB16CE

TC = Qz•Q(z-1)•Q(z-2)•...•Q0

CEO = TC•CE

Figure 4-1CB8CE Implementation XC3000, XC4000, XC5200, Spartans, Virtex

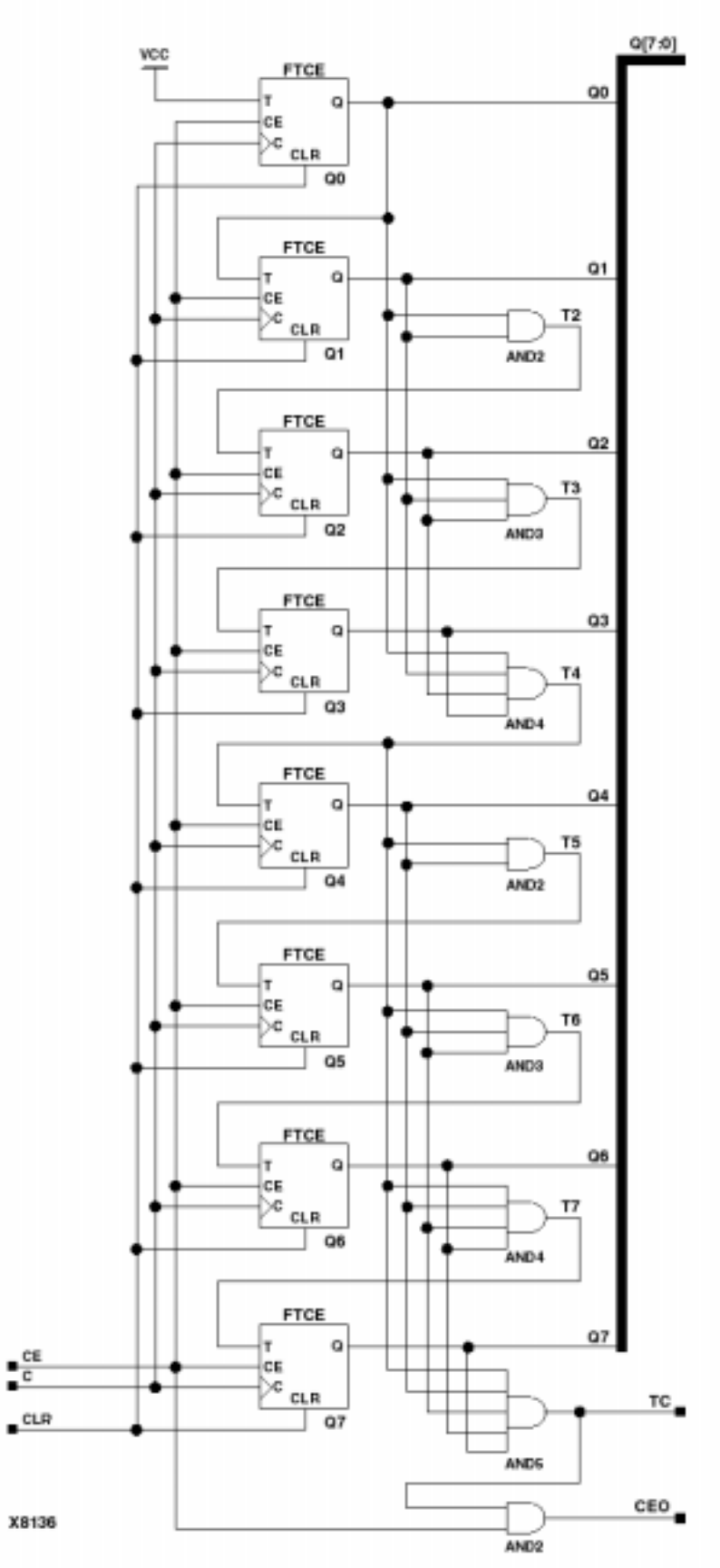

VCC
FTCE
T
CE
C
CLR
Q
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q[7:0]
T2
T3
T4
T5
T6
T7
AND2
AND3
AND4
AND5
CE
C
CLR
TC
CEO
X8136

Figure 4-2CB2CE Implementation XC9000

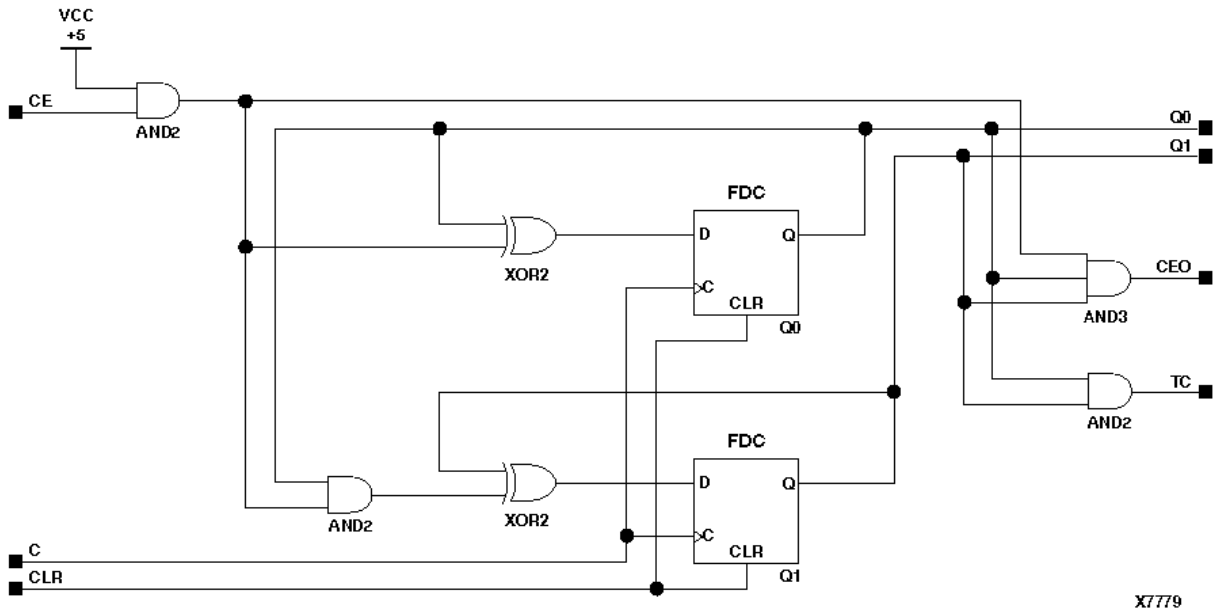
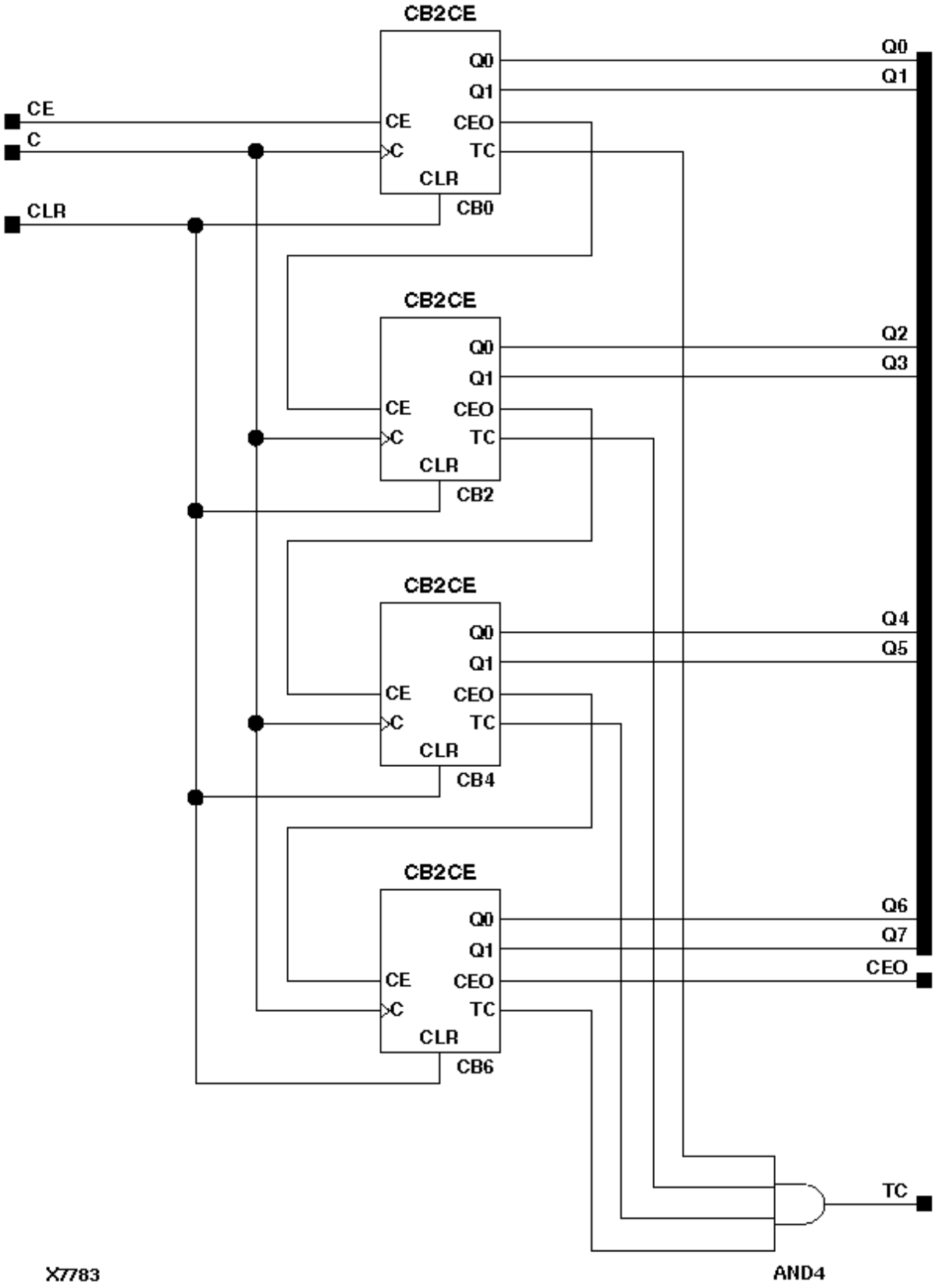


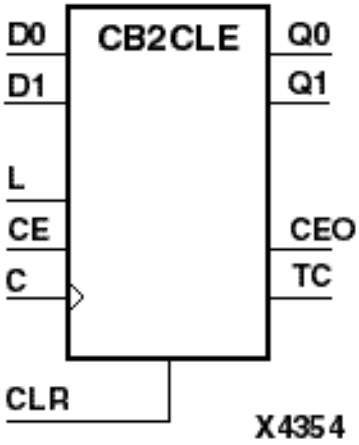
Figure 4-3CB8CE Implementation XC9000

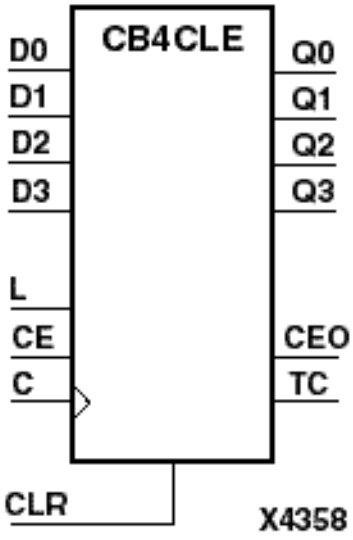

CB2CE
Q0
Q1
CE
CEO
C
TC
CLR
CB0
CE
C
CLR
CB2CE
Q2
Q3
CB2
CB2CE
Q4
Q5
CB4
CB2CE
Q6
Q7
CEO
CB6
TC
X7783
AND4

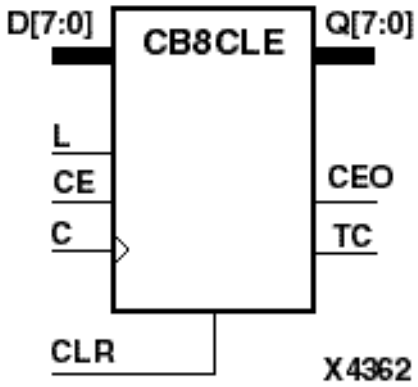
CB2CLE, CB4CLE, CB8CLE, CB16CLE

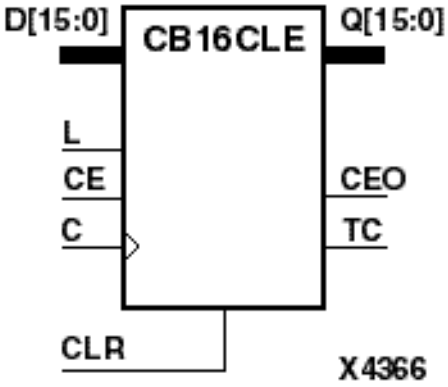
2-, 4-, 8-, 16-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro









CB2CLE, CB4CLE, CB8CLE, and CB16CLE are, respectively, 2-, 4-, 8-, and 16-bit (stage) synchronously loadable, asynchronously clearable, cascadable binary counters. The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Larger counters are created by connecting the CEO output of the first stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE\text{-}TC})$, where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input; use the TC output if it does not.

The counter is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs					Outputs		
CLR	**L**	**CE**	**C**	**Dz – D0**	**Qz – Q0**	**TC**	**CEO**
1	X	X	X	X	0	0	0
0	1	X	↑	Dn	dn	TC	CEO
0	0	0	X	X	No Chg	No Chg	0
0	0	1	↑	X	Inc	TC	CEO

z= 1 for CB2CLE; z = 3 for CB4CLE; z = 7 for CB8CLE; z = 15 for CB16CLE

dn = state of referenced input (Dn) one setup time prior to active clock transition.

TC = Qz•Q(z-1)•Q(z-2)•...•Q0

CEO = TC•CE

Figure 4-4CB8CLE Implementation XC3000

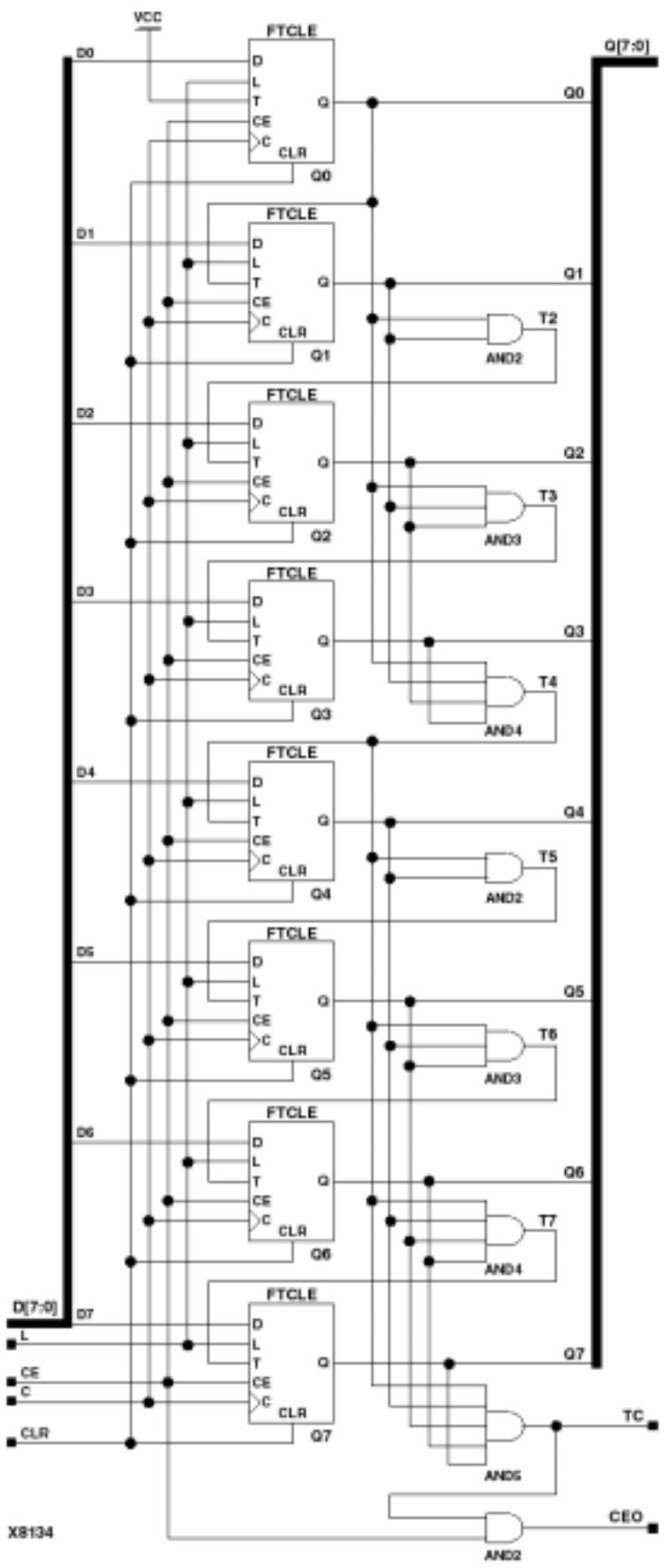

VCC
FTCLE
D0
Q[7:0]
Q0
D
L
T
CE
C
CLR
Q
Q0
D1
Q1
T2
AND2
Q1
D2
Q2
T3
AND3
Q2
D3
Q3
T4
AND4
Q3
D4
Q4
T5
AND2
Q4
D5
Q5
T6
AND3
Q5
D6
Q6
T7
AND4
Q6
D[7:0]
D7
Q7
TC
AND5
CEO
AND2
X8134

Figure 4-5CB8CLE Implementation XC4000, XC5200, Spartans, Virtex

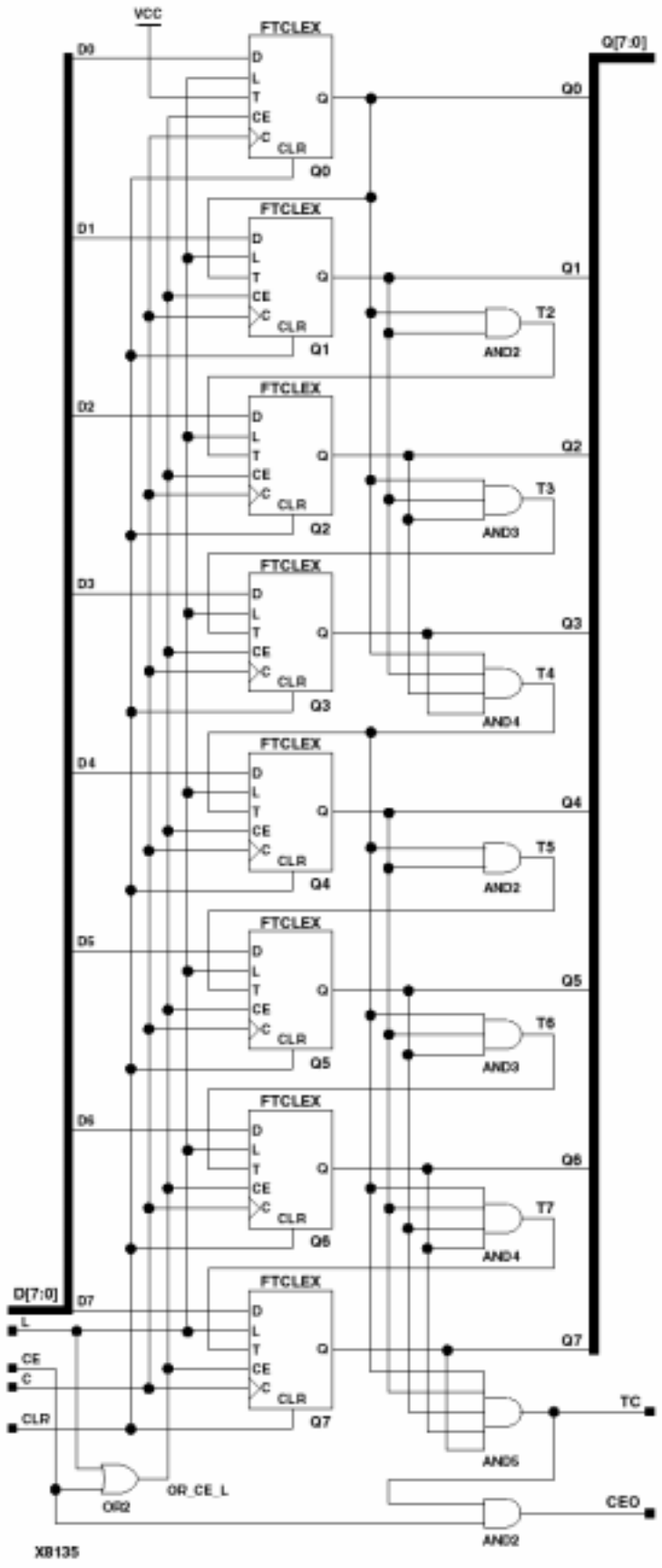

VCC
FTCLEX
D0
Q0
Q[7:0]
D1
Q1
T2
AND2
D2
Q2
T3
AND3
D3
Q3
T4
AND4
D4
Q4
T5
AND2
D5
Q5
T6
AND3
D6
Q6
T7
AND4
D[7:0]
D7
Q7
L
CE
C
CLR
TC
AND5
OR2
OR_CE_L
CEO
AND2
X8135

Figure 4-6CB2CLE Implementation XC9000

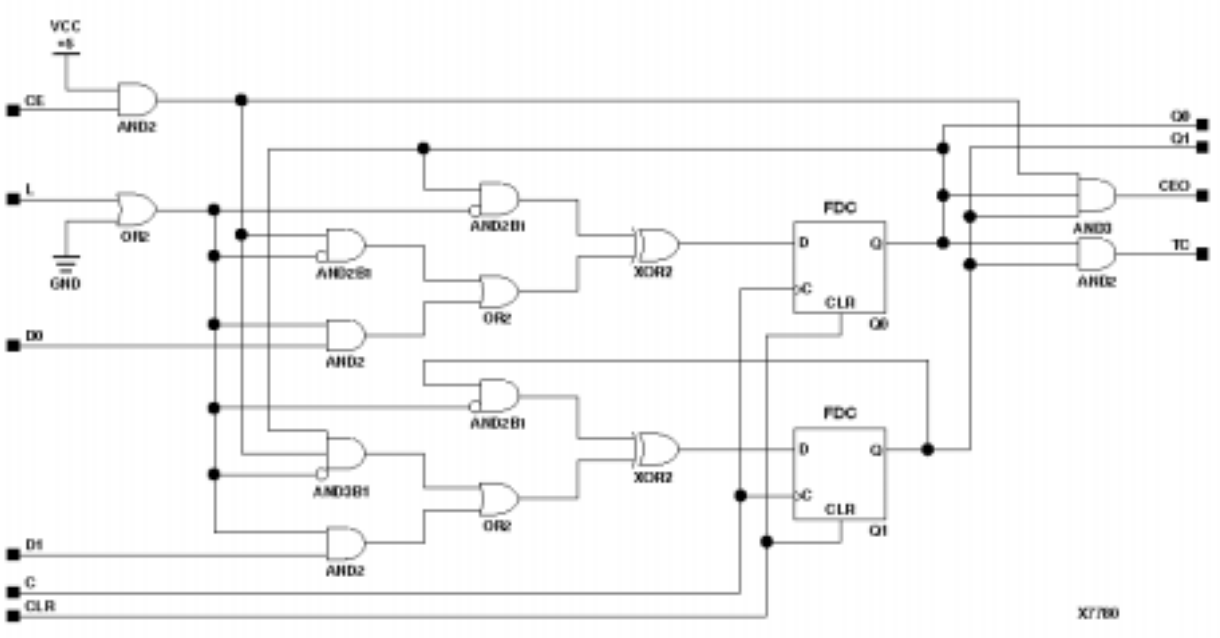
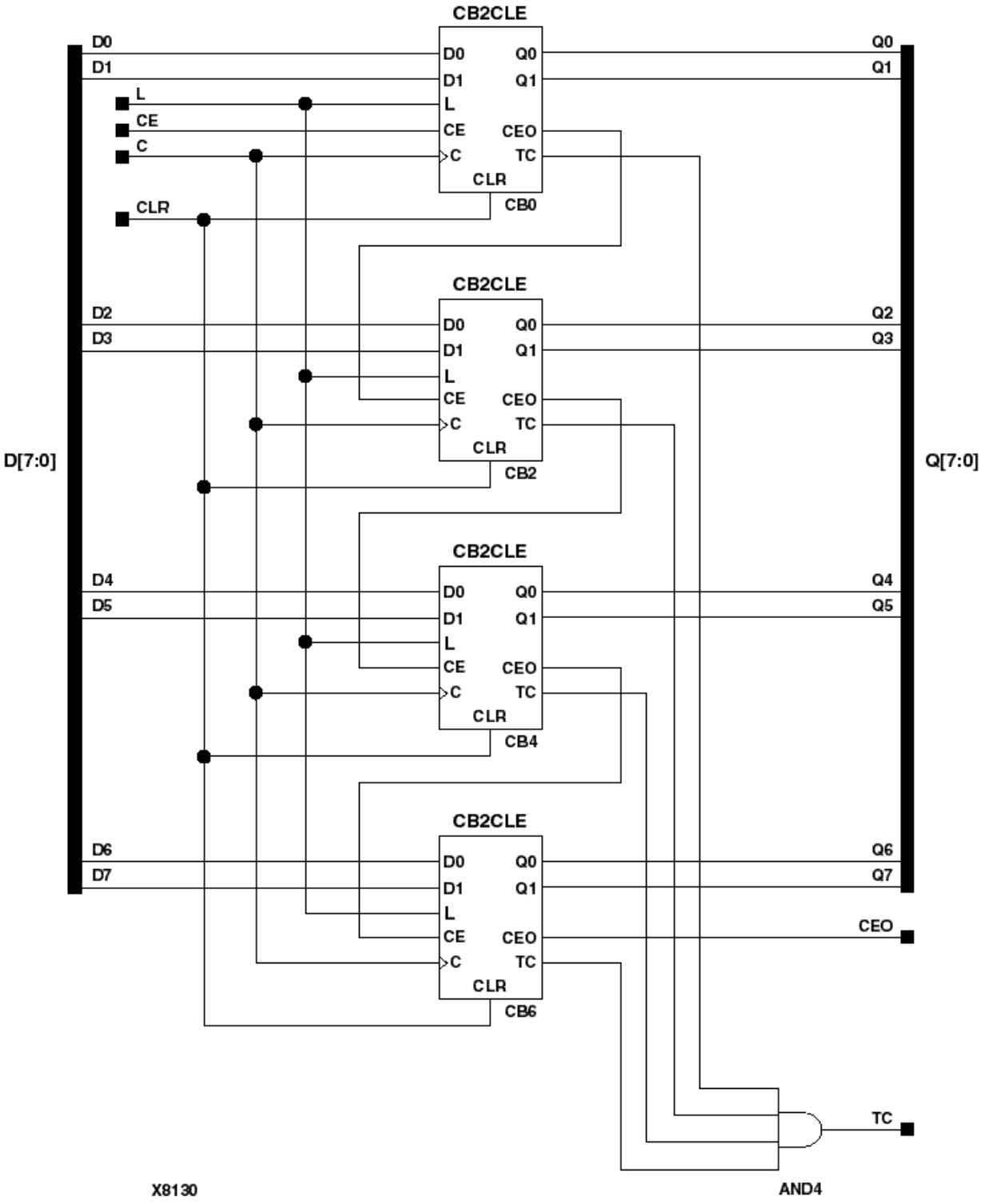


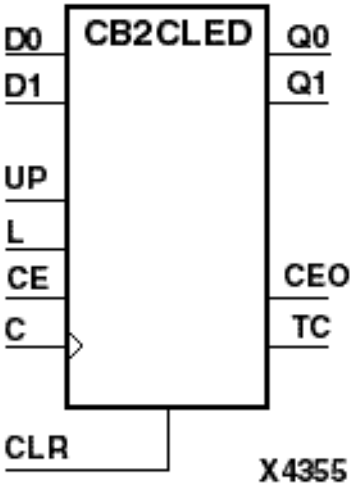
Figure 4-7CB8CLE Implementation XC9000

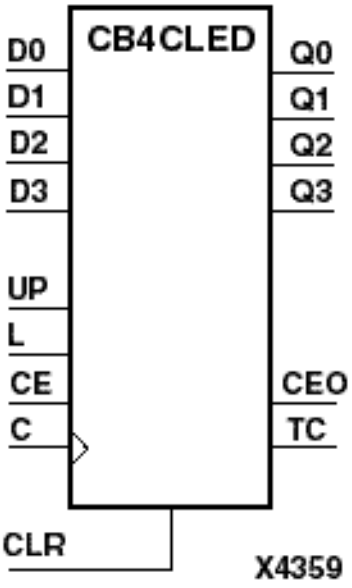


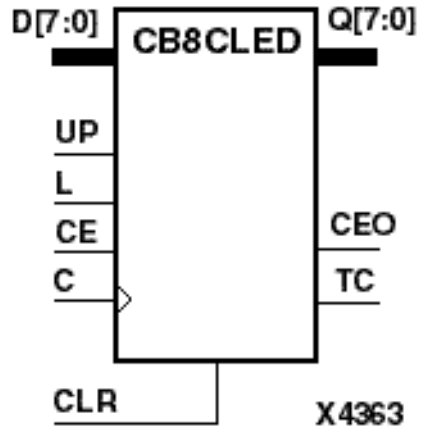
CB2CLED, CB4CLED, CB8CLED, CB16CLED

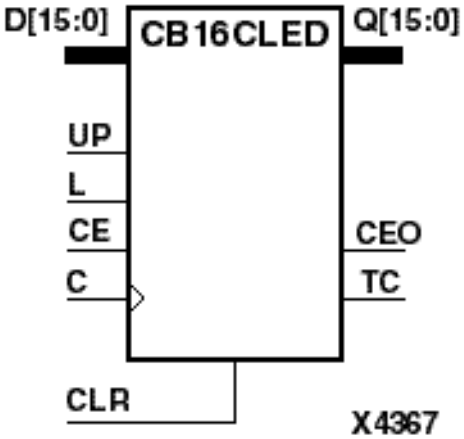
2-, 4-, 8-, 16-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro









CB2CLED, CB4CLED, CB8CLED, and CB16CLED are, respectively, 2-, 4-, 8- and 16-bit (stage), synchronously loadable, asynchronously clearable, cascadable, bidirectional binary counters. The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to-High clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low. To cascade counters, the CEO output of each counter is connected to the CE pin of the next stage. The clock, UP, L, and CLR inputs are connected in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE\text{-}TC})$, where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage.

When cascading counters, use the CEO output if the counter uses the CE input; use the TC output if it does not. For CPLD designs, refer to the **"CB2X1, CB4X1, CB8X1, CB16X1"** section for high-performance cascadable, bidirectional counters.

The counter is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be

simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs						Outputs		
CLR	**L**	**CE**	**C**	**UP**	**Dz – D0**	**Qz – Q0**	**TC**	**CEO**
1	X	X	X	X	X	0	0	0
0	1	X	↑	X	Dn	dn	TC	CEO
0	0	0	X	X	X	No Chg	No Chg	0
0	0	1	↑	1	X	Inc	TC	CEO
0	0	1	↑	0	X	Dec	TC	CEO

z = 1 for CB2CLED; z = 3 for CB4CLED; z = 7 for CB8CLED; z = 15 for CB16CLED

dn = state of referenced input (Dn), one setup time prior to active clock transition

TC = (Qz•Q(z-1)•Q(z-2)•...•Q0•UP) + ($\overline{Qz}$•$\overline{Q(z-1)}$•$\overline{Q(z-2)}$•...•$\overline{Q0}$•$\overline{UP}$)

CEO = TC•CE

Figure 4-8CB8CLED Implementation XC3000

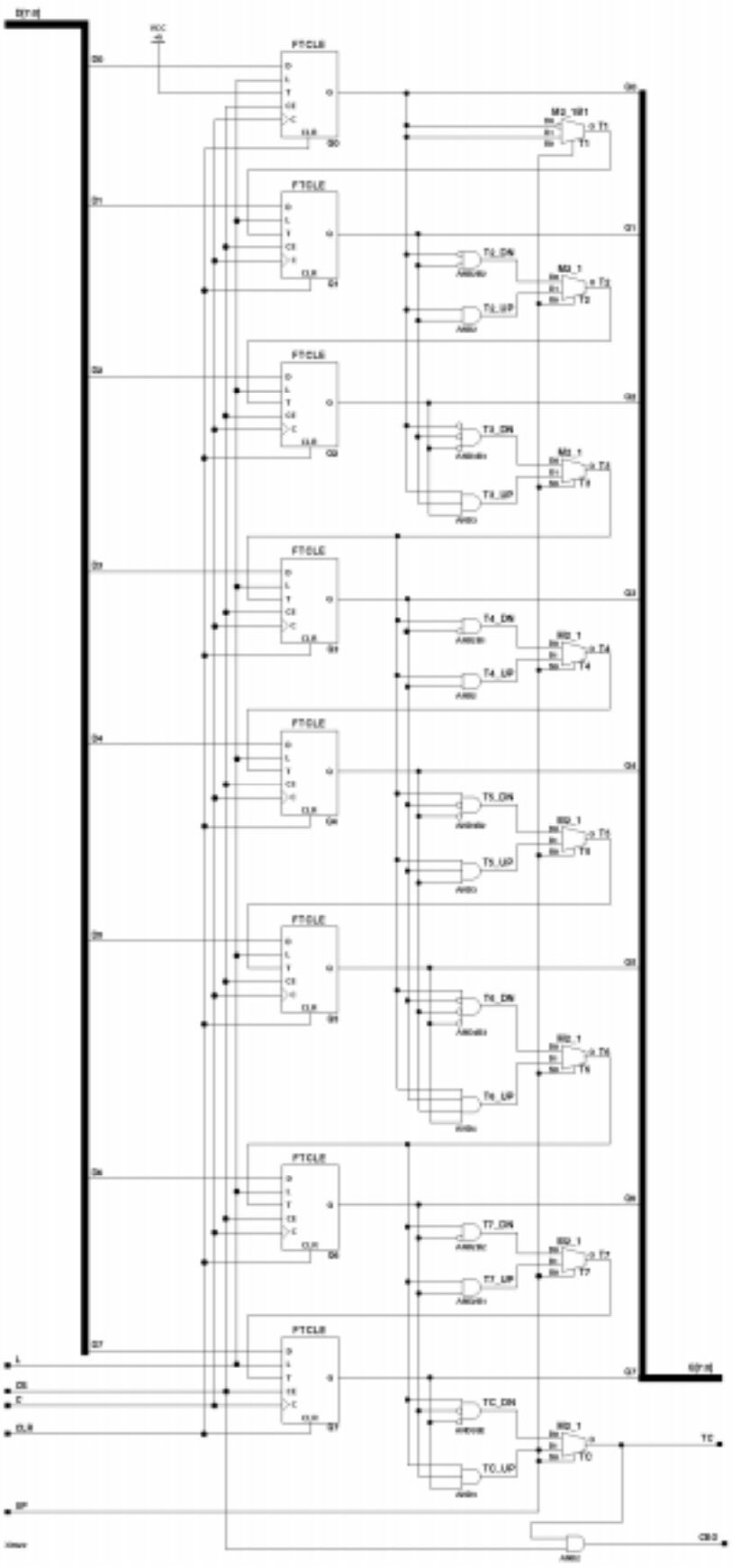

FTCLE
T1
T2
T3
T4
T5
T6
T7
T0
T1_DN
T1_UP
T2_DN
T2_UP
T3_DN
T3_UP
T4_DN
T4_UP
T5_DN
T5_UP
T6_DN
T6_UP
T7_DN
T7_UP
TC_DN
TC_UP
TC
CEO

Figure 4-9CB8CLED Implementation XC4000, XC5200, Spartans, Virtex

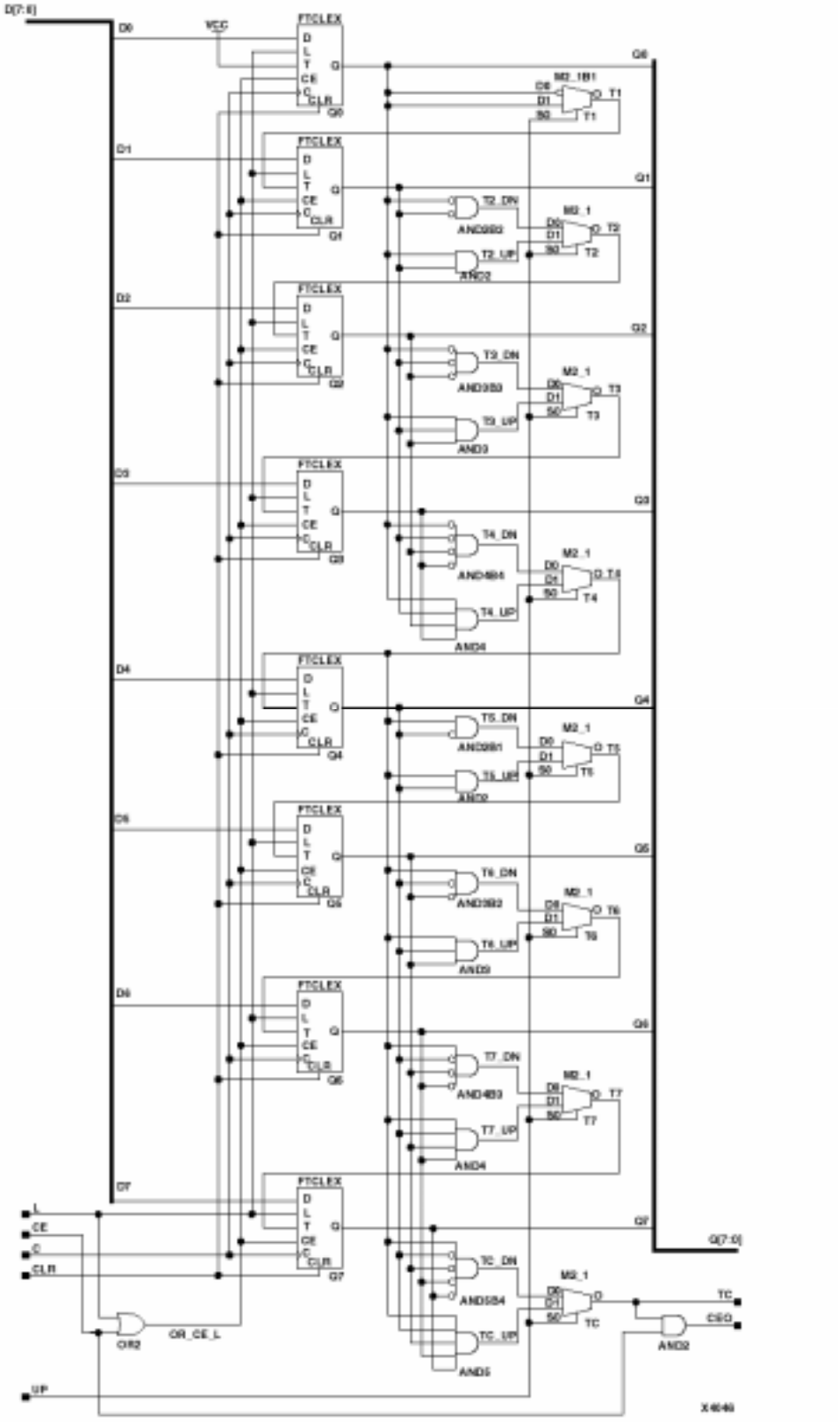
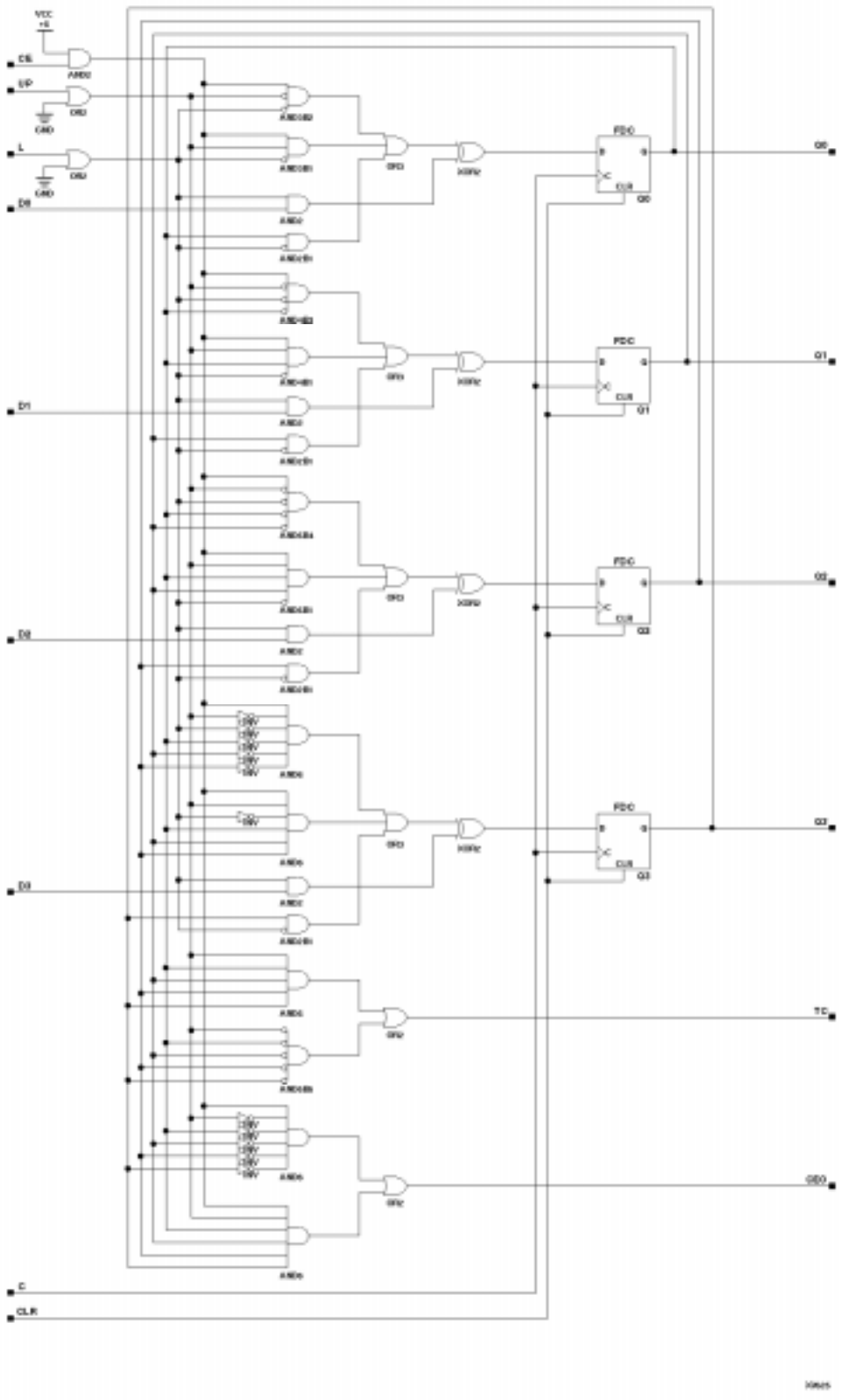

D[7:0]
D0
VCC
FTCLEX
Q0
M2_1B1
T1
D1
Q1
T2_DN
AND2B3
M2_1
T2
T2_UP
AND2
D2
Q2
T3_DN
AND3B3
T3
T3_UP
AND3
D3
Q3
T4_DN
AND4B4
T4
T4_UP
AND4
D4
Q4
T5_DN
AND2B1
T5
T5_UP
AND2
D5
Q5
T6_DN
AND3B2
T6
T6_UP
AND3
D6
Q6
T7_DN
AND4B3
T7
T7_UP
AND4
D7
Q7
Q[7:0]
L
CE
C
CLR
OR2
OR_CE_L
TC_DN
AND5B4
TC
TC_UP
AND5
CEO
AND2
UP
X4646

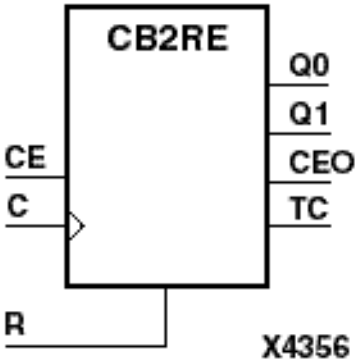
Figure 4-10CB4CLED Implementation XC9000

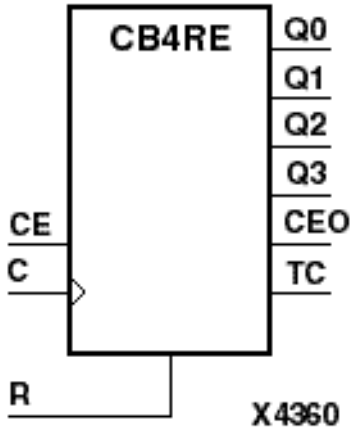

VCC
+5
CE
UP
GND
L
GND
D0
D1
D2
D3
C
CLR
Q0
Q1
Q2
Q3
TC
CEO

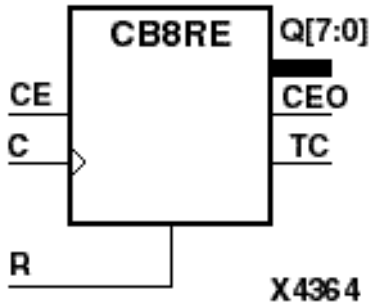
CB2RE, CB4RE, CB8RE, CB16RE

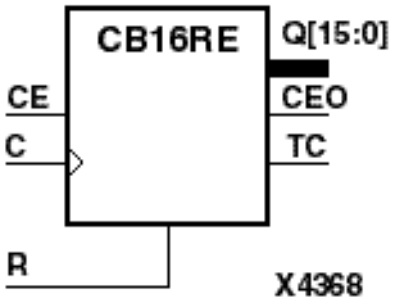
2-, 4-, 8-, 16-Bit Cascadable Binary Counters with Clock Enable and Synchronous Reset

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro









CB2RE, CB4RE, CB8RE, and CB16RE are, respectively, 2-, 4-, 8-, and 16-bit (stage), synchronous, resettable, cascadable binary counters. The synchronous reset (R) is the highest priority input. When R is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero during the Low-to-High clock transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when both Q outputs are High.

Larger counters are created by connecting the CEO output of the first stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE\text{-}TC})$, where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input; use the TC output if it does not.

The counter is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs				**Outputs**	
R	**CE**	**C**	**Qz – Q0**	**TC**	**CEO**
1	X	↑	0	0	0
0	0	X	No Chg	No Chg	0

0	1	↑	Inc	TC	CEO

z = 1 for CB2RE; z = 3 for CB4RE; z = 7 for CB8RE; z = 15 for CB16RE

TC = Qz•Q(z-1)•Q(z-2)•...•Q0)

CEO = TC•CE

Figure 4-11CB8RE Implementation XC3000, XC4000, XC5200, Spartans, Virtex

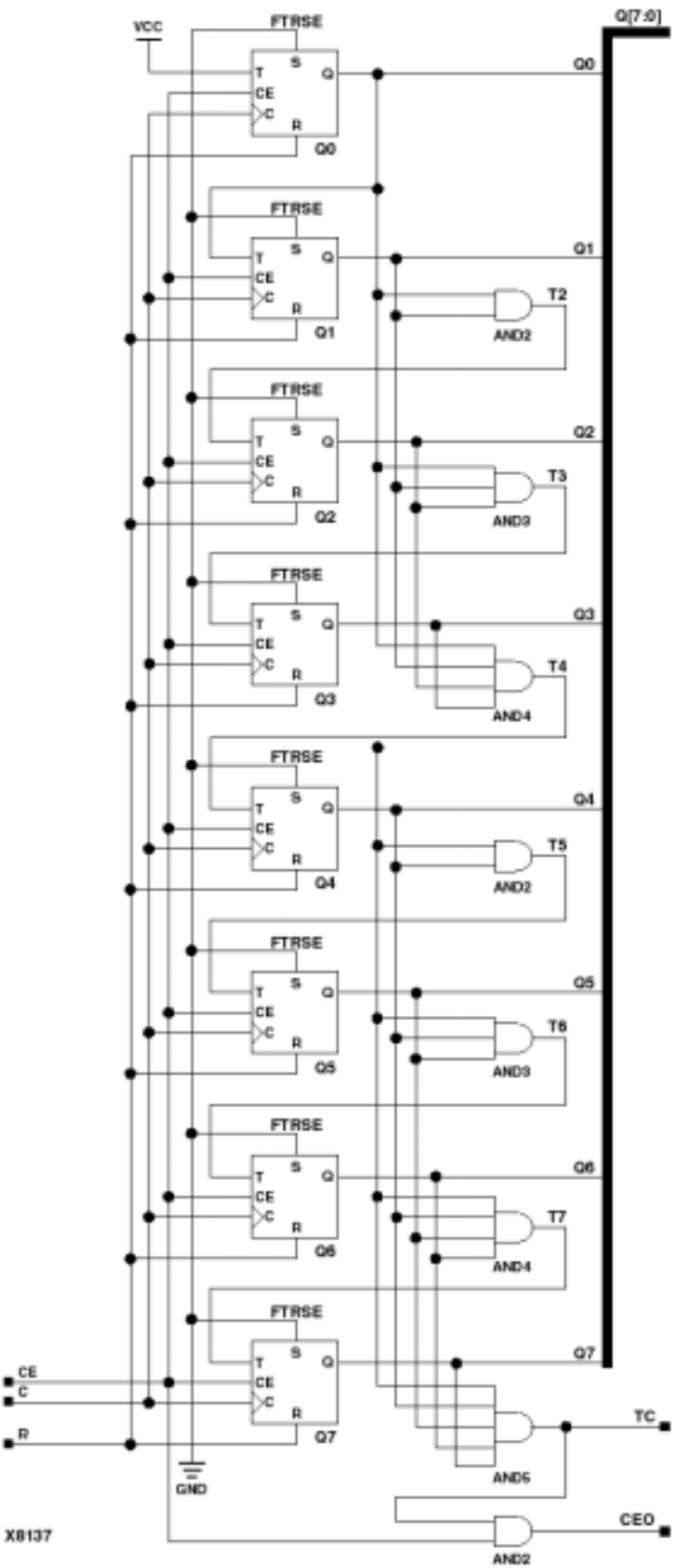

VCC
FTRSE
Q[7:0]
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
T2
T3
T4
T5
T6
T7
T8
AND2
AND3
AND4
AND5
TC
CEO
CE
C
R
GND
X8137

Figure 4-12CB2RE Implementation XC9000

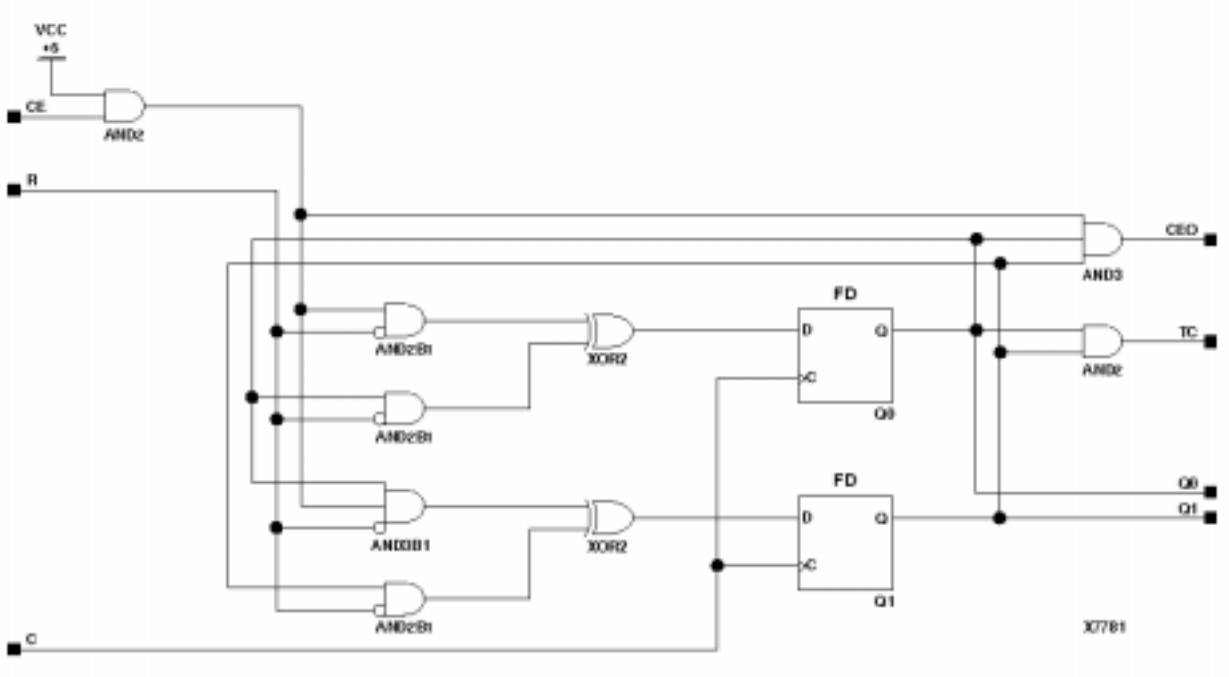
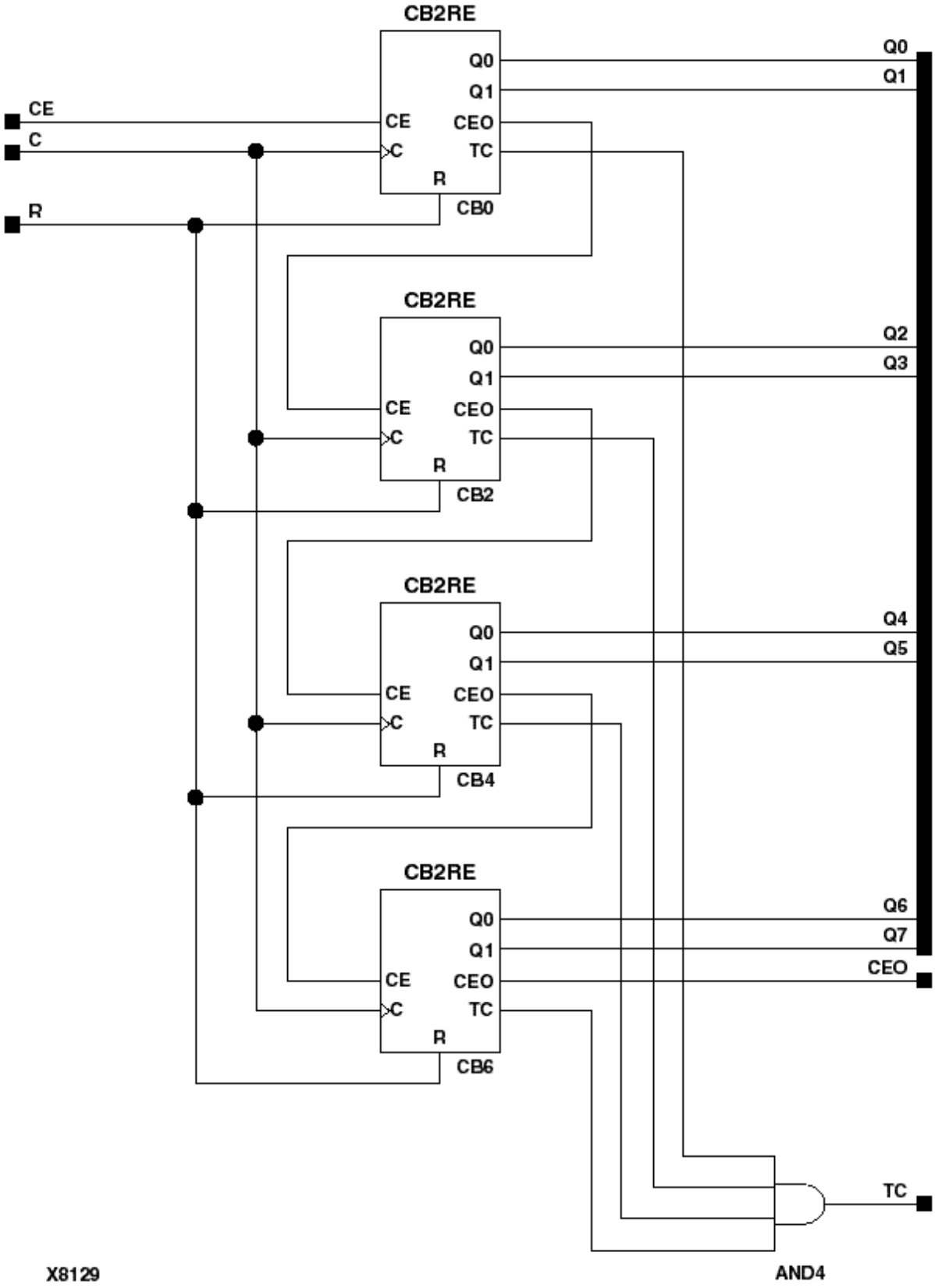


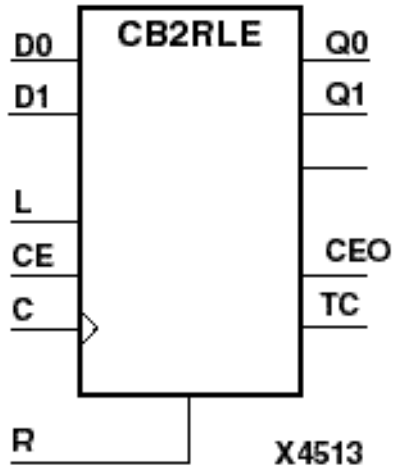
Figure 4-13CB8RE Implementation XC9000

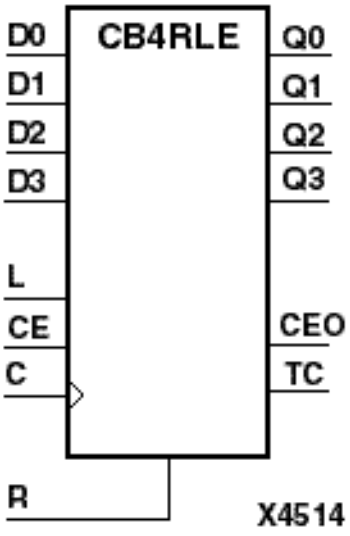

CB2RE
Q0
Q1
CE
CEO
C
TC
R
CB0
CE
C
R
CB2RE
Q2
Q3
CB4
CB2RE
Q4
Q5
CB6
CB2RE
Q6
Q7
CEO
TC
AND4
X8129

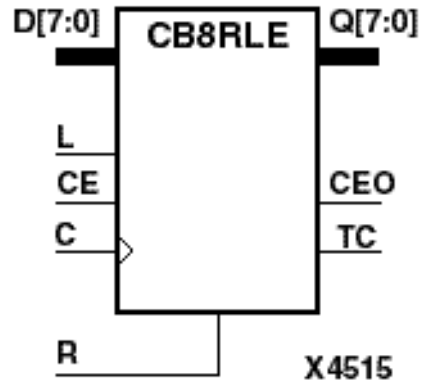
CB2RLE, CB4RLE, CB8RLE, CB16RLE

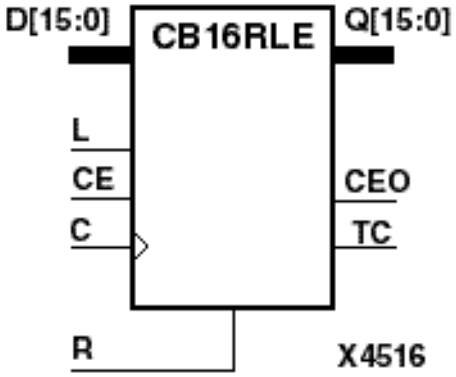
2-, 4-, 8-, 16-Bit Loadable Cascadable Binary Counters with Clock Enable and Synchronous Reset

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	N/A	N/A	Macro	N/A	N/A	N/A









CB2RLE, CB4RLE, CB8RLE, and CB16RLE are, respectively, 2-, 4-, 8-, and 16-bit (stage), synchronous, loadable, resettable, cascadable binary counter. The synchronous reset (R) is the highest priority input. The synchronous R, when High, overrides all other inputs and resets the Q outputs, terminal count (TC), and clock enable out (CEO) outputs to Low on the Low-to-High clock (C) transition.

The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of CE. The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High. The CEO output is High when all Q outputs and CE are High to allow direct cascading of counters.

Larger counters are created by connecting the CEO output of the first stage to the CE input of the next stage and by connecting the C, L, and R inputs in parallel. The maximum length of the counter is determined by the accumulated CE-to-CEO propagation delays versus the clock period. When cascading counters, use the CEO output if the counter uses the CE input; use the TC output if it does not.

The counter is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs					Outputs		
R	L	CE	C	Dz – D0	Qz – Q0	TC	CEO

1	X	X	↑	X	0	0	0
0	1	X	↑	Dn	dn	TC	CEO
0	0	0	X	X	No Chg	No Chg	0
0	0	1	↑	X	Inc	TC	CEO

z = 1 for CB2RLE; z = 3 for CB4RLE; z = 7 for CB8RLE; z = 15 for CB16RLE

dn = state of referenced input (Dn) one setup time prior to active clock transition

TC = Qz•Q(z-1)•Q(z-2)•...•Q0

CEO = TC•CE

Figure 4-14CB2RLE Implementation XC9000

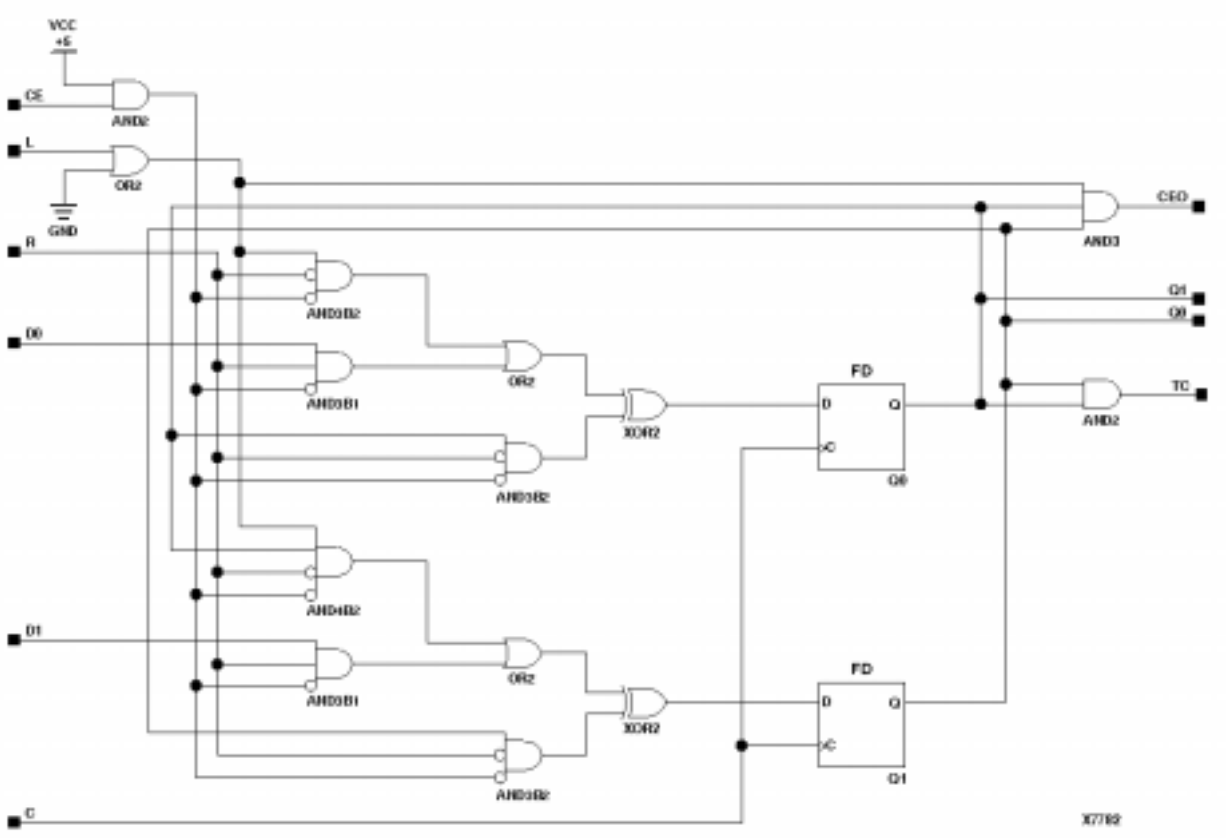
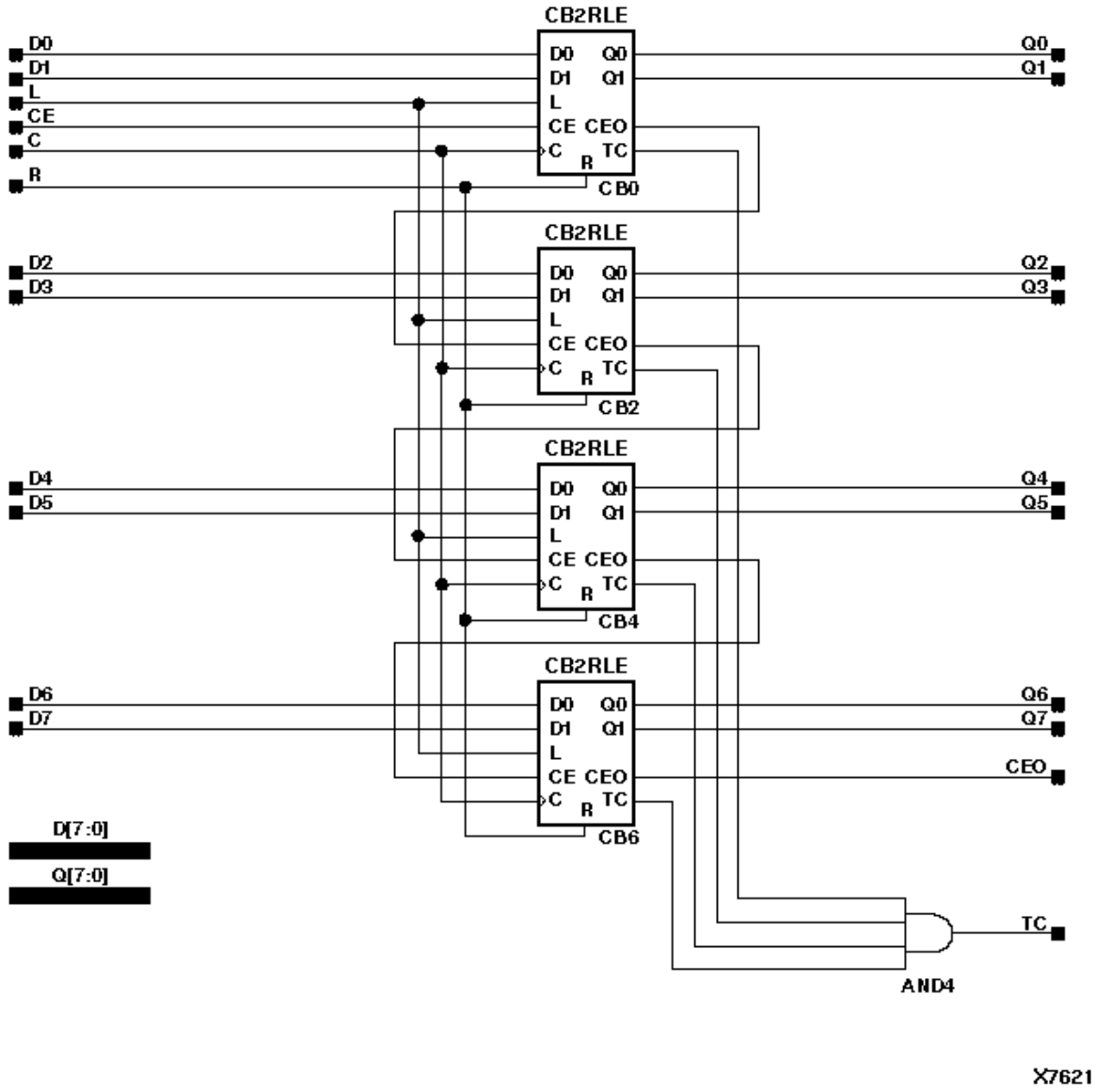


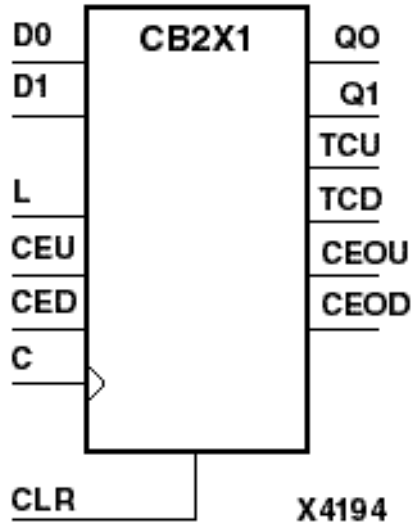
Figure 4-15CB8RLE Implementation XC9000

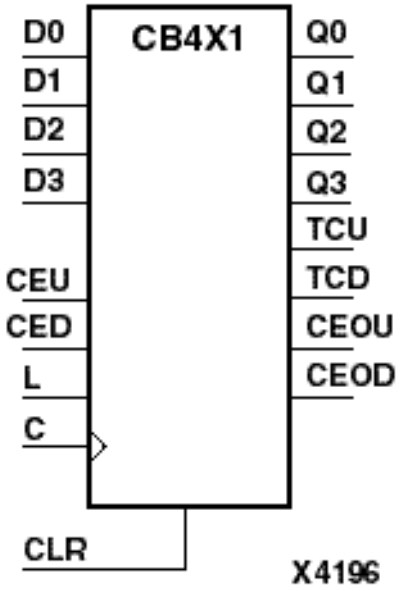


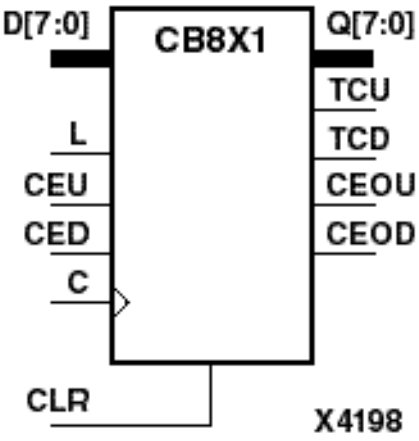
CB2X1, CB4X1, CB8X1, CB16X1

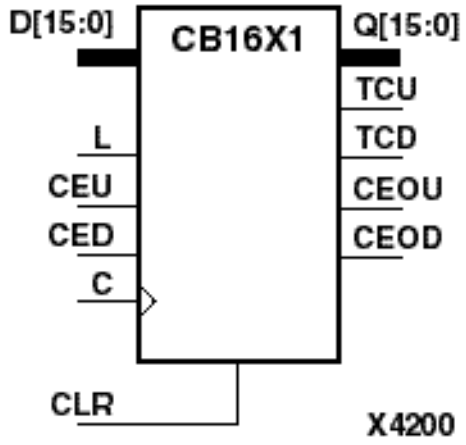
2-, 4-, 8-, 16-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	N/A	N/A	Macro	N/A	N/A	N/A


D0
D1
L
CEU
CED
C
CLR
CB2X1
QO
Q1
TCU
TCD
CEOU
CEOD
X4194


D0
D1
D2
D3
CEU
CED
L
C
CLR
CB4X1
Q0
Q1
Q2
Q3
TCU
TCD
CEOU
CEOD
X4196


D[7:0]
L
CEU
CED
C
CLR
CB8X1
Q[7:0]
TCU
TCD
CEOU
CEOD
X4198



CB2X1, CB4X1, CB8X1, and CB16X1 are, respectively, 2-, 4-, 8-, and 16-bit (stage), synchronously loadable, asynchronously clearable, bidirectional binary counters. These counters have separate count-enable inputs and synchronous terminal-count outputs for up and down directions to support high-speed cascading in the CPLD architecture.

The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; data outputs (Q) go to logic level zero, terminal count outputs TCU and TCD go to zero and one, respectively, clock enable outputs CEOU and CEOD go to Low and High, respectively, independent of clock transitions. The data on the D inputs loads into the counter on the Low-to-High clock (C) transition when the load enable input (L) is High, independent of the CE inputs.

The Q outputs increment when CEU is High, provided CLR and L are Low, during the Low-to-High clock transition. The Q outputs decrement when CED is High, provided CLR and L are Low. The counter ignores clock transitions when CEU and CED are Low. Both CEU and CED should not be High during the same clock transition; the CEOU and CEOD outputs might not function properly for cascading when CEU and CED are both High.

For counting up, the CEOU output is High when all Q outputs and CEU are High. For counting down, the CEOD output is High when all Q outputs are Low and CED is High. To cascade counters, the CEOU and CEOD outputs of each counter are connected directly to the CEU and CED inputs, respectively, of the next stage. The clock, L, and CLR inputs are connected in parallel.

In Xilinx CPLD devices, the maximum clocking frequency of these counter components is unaffected by the number of cascaded stages for all counting and loading functions. The TCU terminal count output is High when all Q outputs are High, regardless of CEU. The TCD output is High when all Q outputs are Low, regardless of CED.

When cascading counters, the final terminal count signals can be produced by AND wiring all the TCU outputs (for the up direction) and all the TCD outputs (for the down direction). The TCU, CEOU, and CEOD outputs are produced by optimizable AND gates within the component, resulting in zero propagation from the CEU and CED inputs and from the Q outputs, provided all connections from each such output remain on-chip. Otherwise, a macrocell buffer delay is introduced.

The counter is initialized to zero (TCU Low and TCD High) when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs	Outputs

CLR	L	CEU	CED	C	Dz–D0	Qz–Q0	TCU	TCD	CEOU	CEOD
1	X	X	X	X	X	0	0	1	0	CEOD
0	1	X	X	↑	Dn	dn	TCU	TCD	CEOU	CEOD
0	0	0	0	X	X	No Chg	No Chg	No Chg	0	0
0	0	1	0	↑	X	Inc	TCU	TCD	CEOU	0
0	0	0	1	↑	X	Dec	TCU	TCD	0	CEOD
0	0	1	1	↑	X	Inc	TCU	TCD	Invalid	Invalid

z = 1 for CB2X1; z = 3 for CB4X1; z = 7 for CB8X1; z = 15 for CB16X1

dn = state of referenced input (Dn) one setup time prior to active clock transition

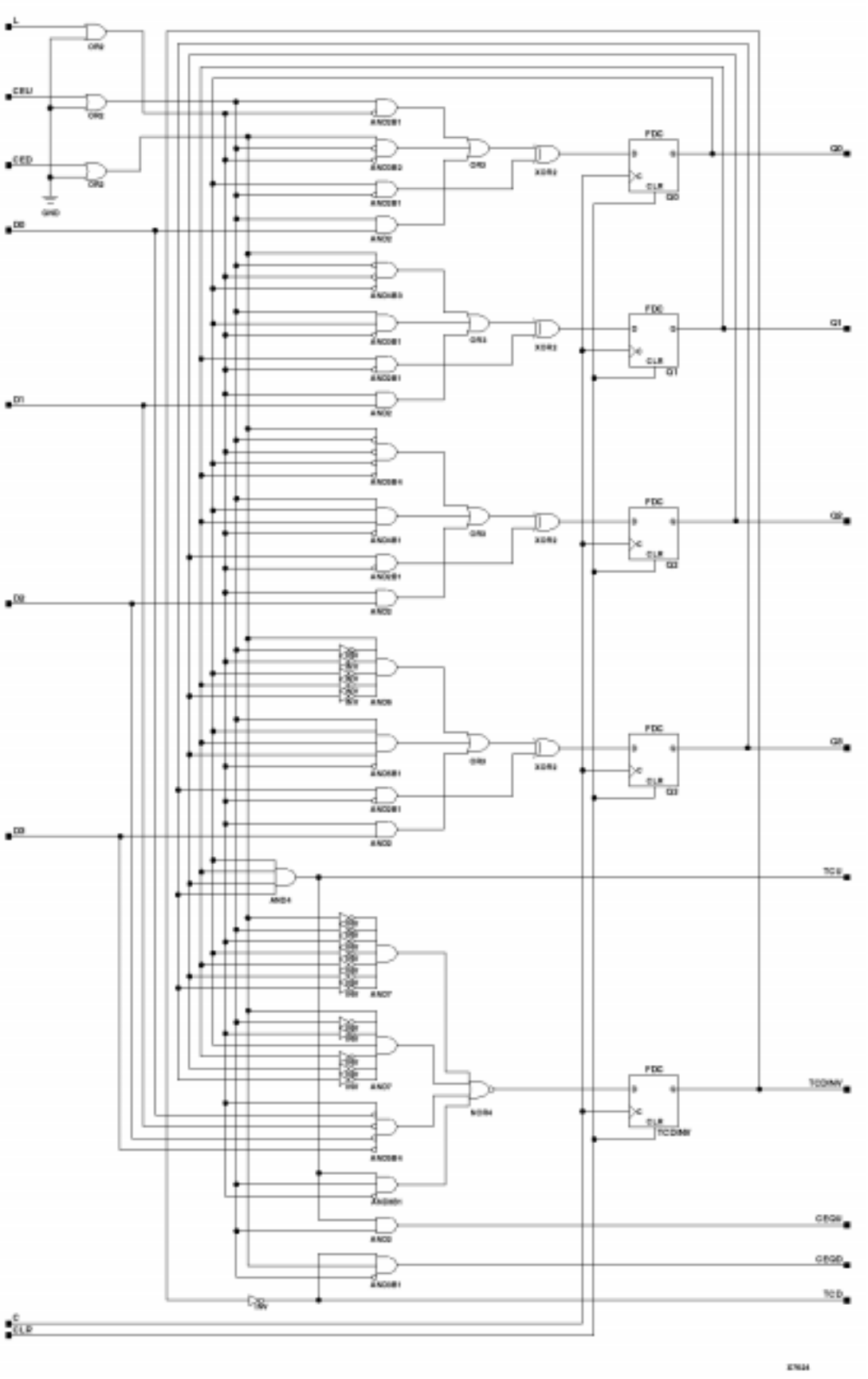
TCU = $Qz \bullet Q(z-1) \bullet Q(z-2) \bullet ... \bullet Q0$

TCD = $\overline{Qz} \bullet \overline{Q(z-1)} \bullet \overline{Q(z-2)} \bullet ... \bullet \overline{Q0}$

CEOU = TCU•CEU

CEOD = TCD•CED

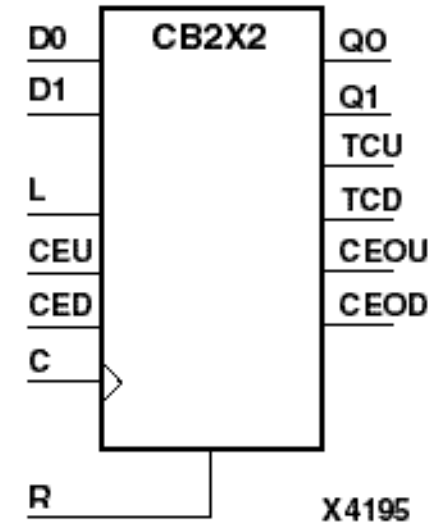
Figure 4-16CB4X1 Implementation XC9000

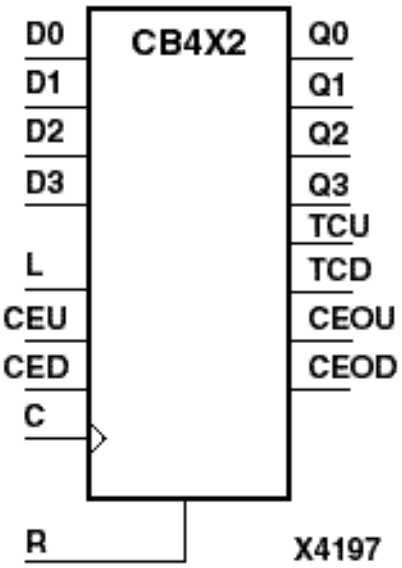


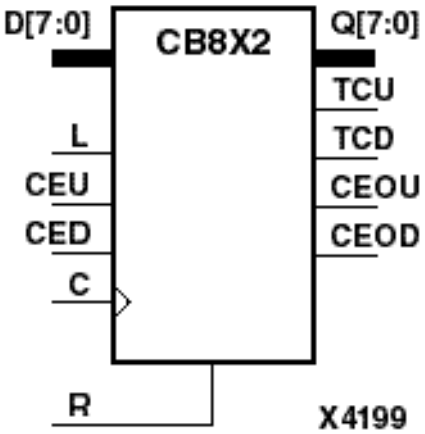
CB2X2, CB4X2, CB8X2, CB16X2

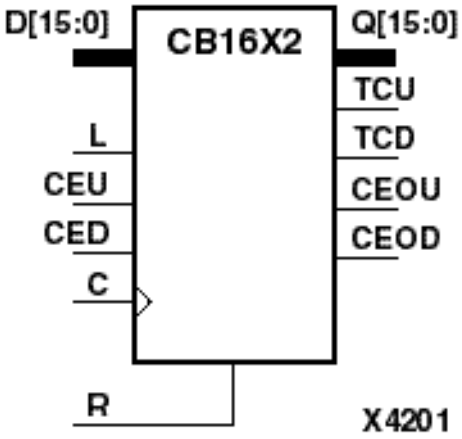
2-, 4-, 8-, and 16-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Synchronous Reset

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	N/A	N/A	Macro	N/A	N/A	N/A









CB2X2, CB4X2, CB8X2, and CB16X2 are, respectively, 2-, 4-, 8-, and 16-bit (stage), synchronous, loadable, resettable, bidirectional binary counters. These counters have separate count-enable inputs and synchronous terminal-count outputs for up and down directions to support high-speed cascading in the CPLD architecture.

The synchronous reset (R) is the highest priority input. When R is High, all other inputs are ignored; the data outputs (Q) go to logic level zero, terminal count outputs TCU and TCD go to zero and one, respectively, and clock enable outputs CEOU and CEOD go to Low and High, respectively, on the Low-to-High clock (C) transition. The data on the D inputs loads into the counter on the Low-to-High clock (C) transition when the load enable input (L) is High, independent of the CE inputs.

All Q outputs increment when CEU is High, provided R and L are Low during the Low-to-High clock transition. All Q outputs decrement when CED is High, provided R and L are Low. The counter ignores clock transitions when CEU and CED are Low. Both CEU and CED should not be High during the same clock transition; the CEOU and CEOD outputs might not function properly for cascading when CEU and CED are both High.

For counting up, the CEOU output is High when all Q outputs and CEU are High. For counting down, the CEOD output is High when all Q outputs are Low and CED is High. To cascade counters, the CEOU and CEOD outputs of each counter are, respectively, connected directly to the CEU and CED inputs of the next stage. The C, L, and R inputs are connected in parallel.

In Xilinx CPLD devices, the maximum clocking frequency of these counter components is unaffected by the number of cascaded stages for all counting and loading functions. The TCU terminal count output is High when all Q outputs are

High, regardless of CEU. The TCD output is High when all Q outputs are Low, regardless of CED.

When cascading counters, the final terminal count signals can be produced by AND wiring all the TCU outputs (for the up direction) and all the TCD outputs (for the down direction). The TCU, CEOU, and CEOD outputs are produced by optimizable AND gates within the component, resulting in zero propagation from the CEU and CED inputs and from the Q outputs, provided all connections from each such output remain on-chip. Otherwise, a macrocell buffer delay is introduced.

The counter is initialized to zero (TCU Low and TCD High) when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net.

Inputs						Outputs				
R	**L**	**CEU**	**CED**	**C**	**Dz – D0**	**Qz – Q0**	**TCU**	**TCD**	**CEOU**	**CEOD**
1	X	X	X	↑	X	0	0	1	0	CEOD
0	1	X	X	↑	Dn	dn	TCU	TCD	CEOU	CEOD
0	0	0	0	X	X	No Chg	No Chg	No Chg	0	0
0	0	1	0	↑	X	Inc	TCU	TCD	CEOU	0
0	0	0	1	↑	X	Dec	TCU	TCD	0	CEOD
0	0	1	1	↑	X	Inc	TCU	TCD	Invalid	Invalid

z = 1 for CB2X2; z = 3 for CB4X2; z = 7 for CB8X2; z = 15 for CB16X2

d = state of referenced input (Dn) one setup time prior to active clock transition

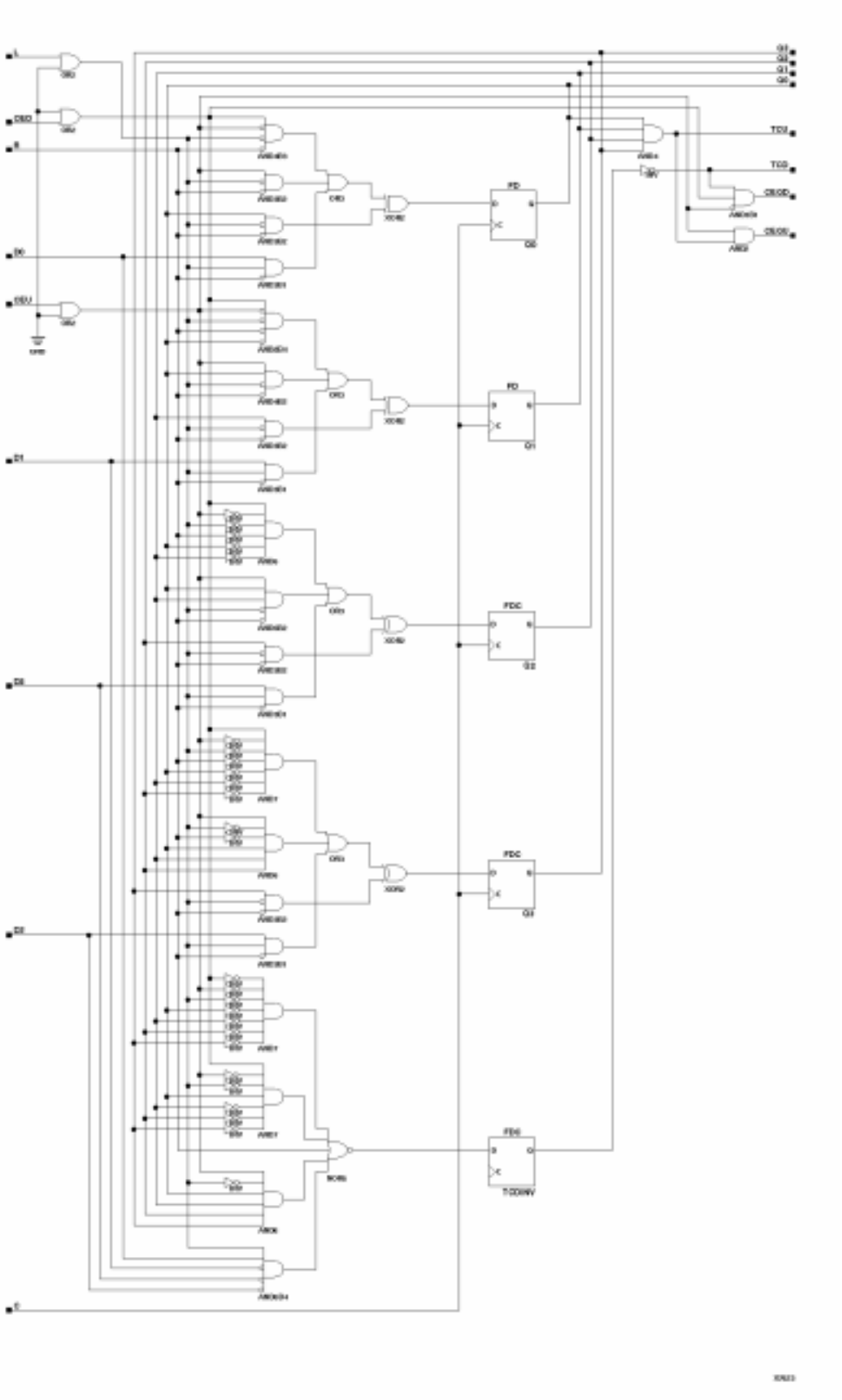
TCU = Qz•Q(z-1)•Q(z-2)•...•Q0

TCD = $\overline{Qz}$•$\overline{Q(z-1)}$•$\overline{Q(z-2)}$•...•$\overline{Q0}$

CEOU = TCU•CEU

CEOD = TCD•CED

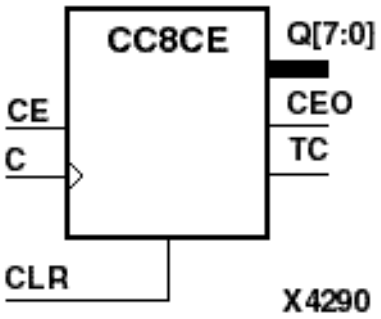
Figure 4-17CB4X2 Implementation XC9000

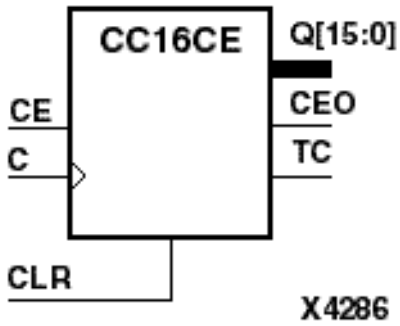


CC8CE, CC16CE

8-, 16-Bit Cascadable Binary Counters with Clock Enable and Asynchronous Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	Macro	N/A	Macro	Macro	Macro





CC8CE and CC16CE are, respectively, 8- and 16-bit (stage), asynchronous, clearable, cascadable binary counters. These counters are implemented using carry logic with relative location constraints to ensure efficient placement of logic. The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Larger counters are created by connecting the count enable out (CEO) output of the first stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE\text{-}TC})$, where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input; use the TC output if

it does not.

The counter is asynchronously cleared, with Low outputs, when power is applied. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs			Outputs		
CLR	**CE**	**C**	**Qz – Q0**	**TC**	**CEO**
1	X	X	0	0	0
0	0	X	No Chg	No Chg	0
0	1	↑	Inc	TC	CEO

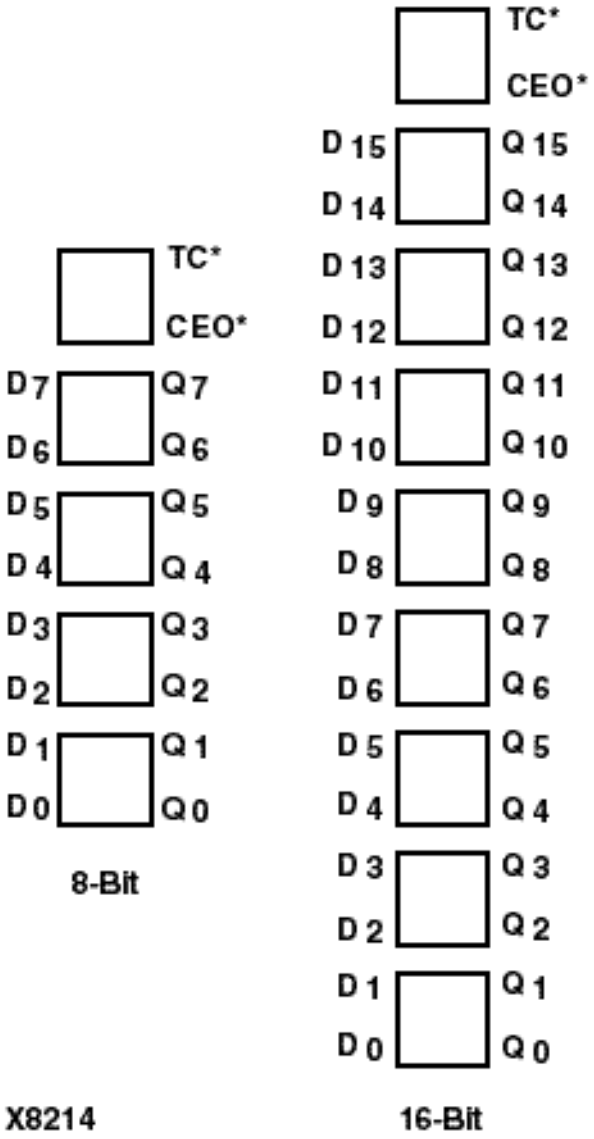
z = 7 for CC8CE; z = 15 for CC16CE

TC = Qz•Q(z-1)•Q(z-2)•...•Q0

CEO = TC•CE

Topology for XC4000 and Spartans

This is the CC8CE (8-bit) and CC16CE (16-bit) topology for XC4000 and Spartan series devices.



Topology for XC5200

This is the CC8CE (8-bit) and CC16CE (16-bit) topology for XC5200 devices.

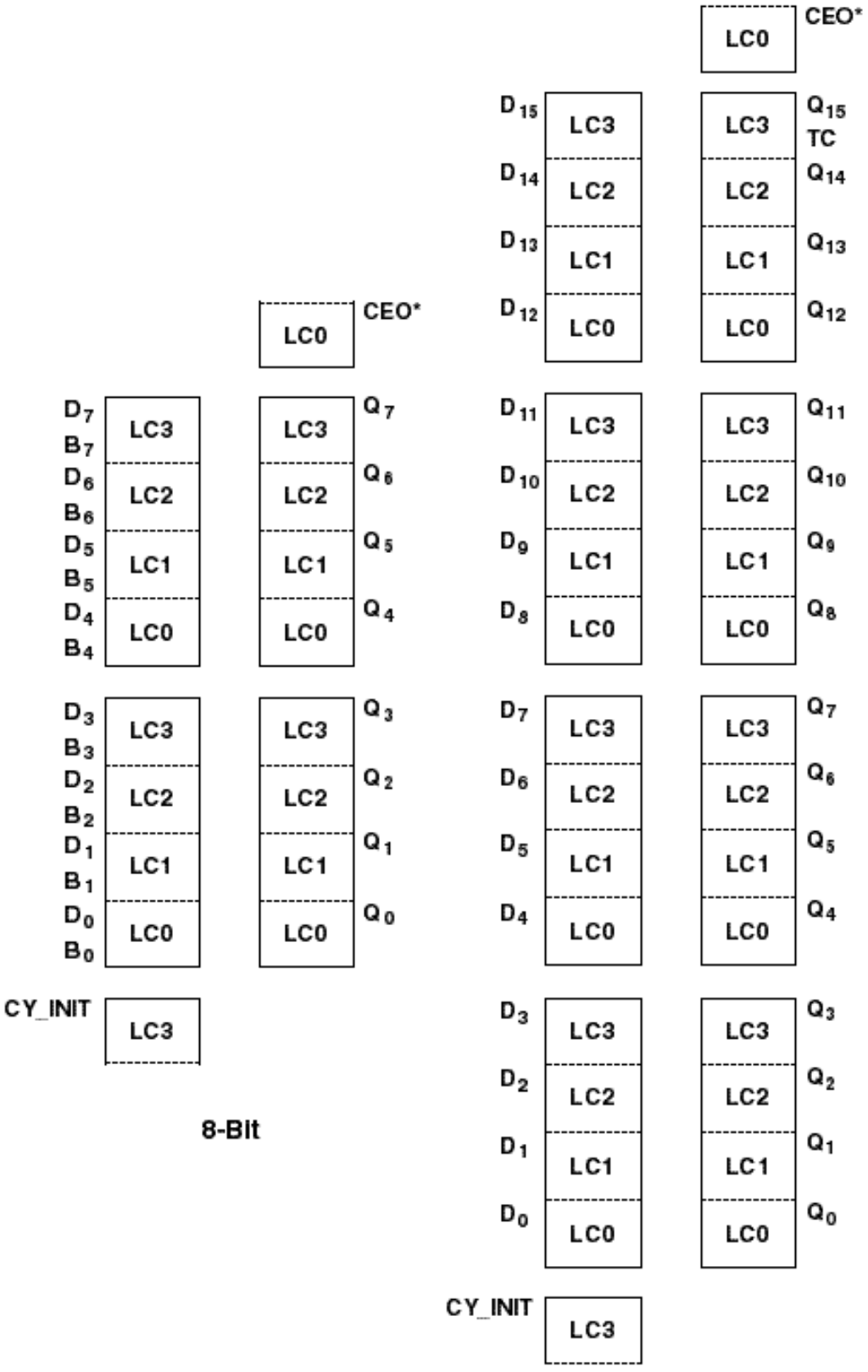

CEO*
LC0
D15
LC3
Q15
TC
D14
LC2
Q14
D13
LC1
Q13
D12
LC0
Q12
CEO*
LC0
D7
B7
LC3
Q7
D6
B6
LC2
Q6
D5
B5
LC1
Q5
D4
B4
LC0
Q4
D11
LC3
Q11
D10
LC2
Q10
D9
LC1
Q9
D8
LC0
Q8
D3
B3
LC3
Q3
D2
B2
LC2
Q2
D1
B1
LC1
Q1
D0
B0
LC0
Q0
D7
LC3
Q7
D6
LC2
Q6
D5
LC1
Q5
D4
LC0
Q4
CY_INIT
LC3
D3
LC3
Q3
D2
LC2
Q2
D1
LC1
Q1
D0
LC0
Q0
CY_INIT
LC3
8-Bit
16-Bit
x8209

Figure 4-18CC8CE Implementation XC4000, Spartans

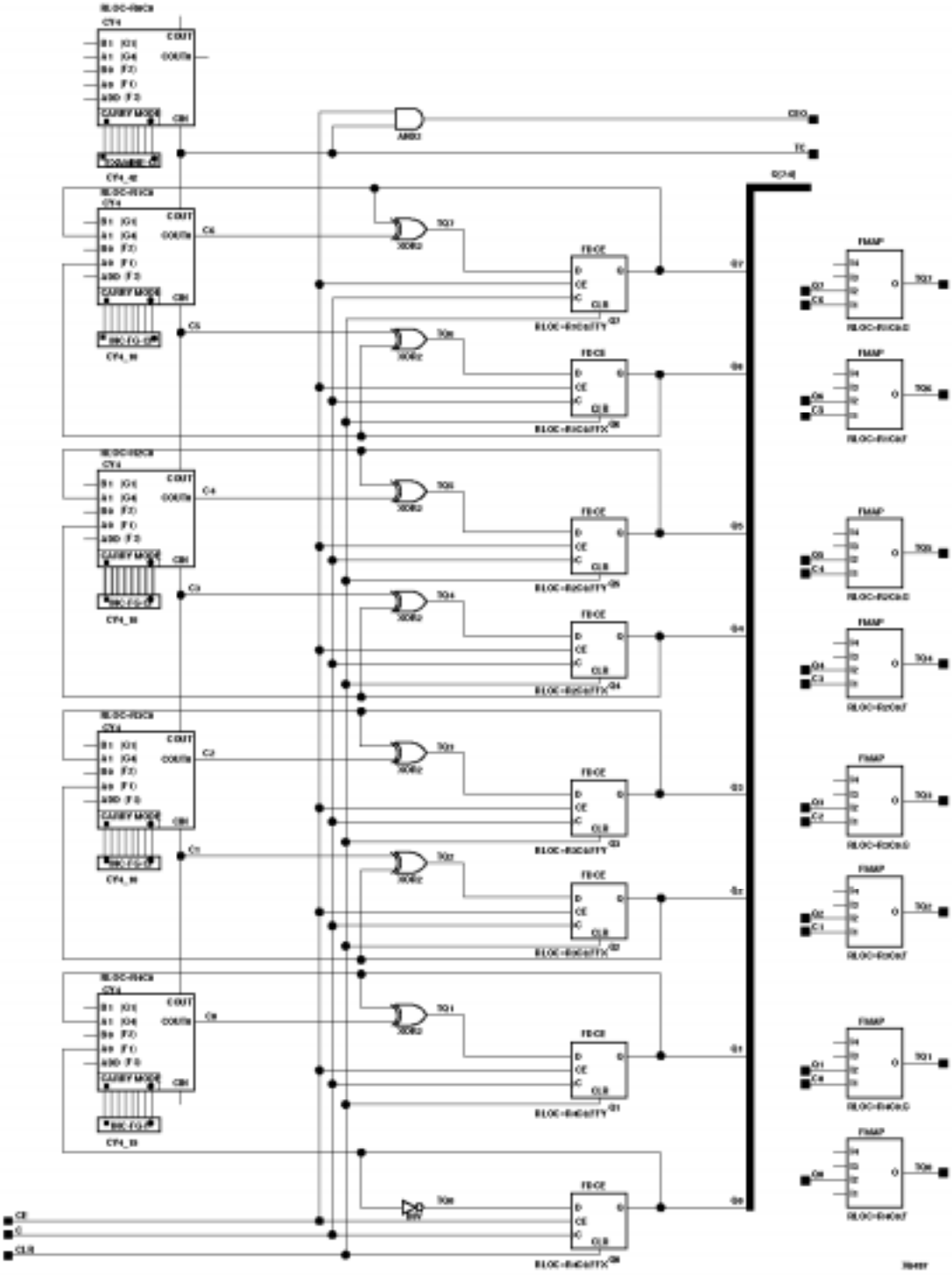


Figure 4-19CC8CE Implementation XC5200

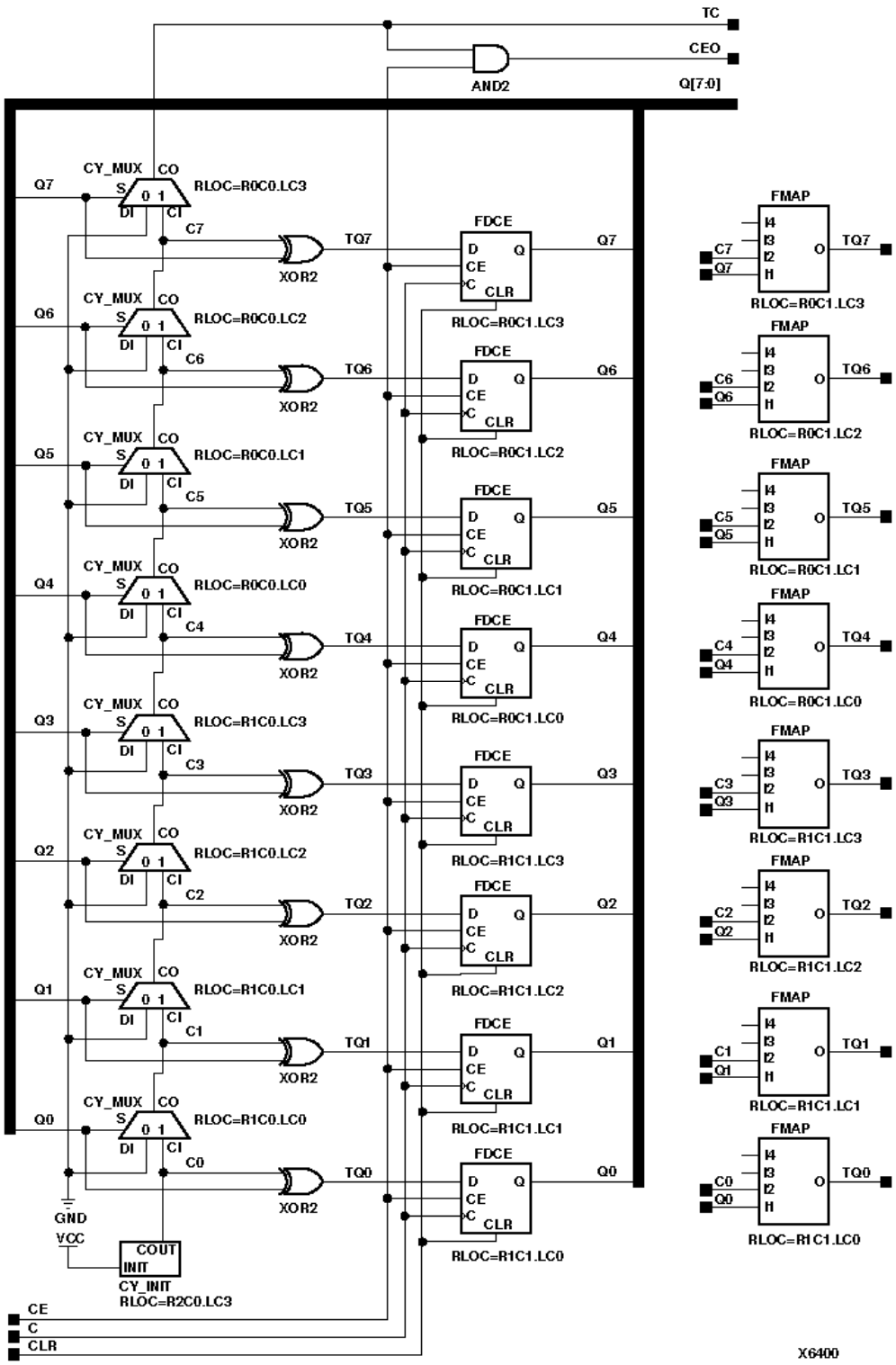
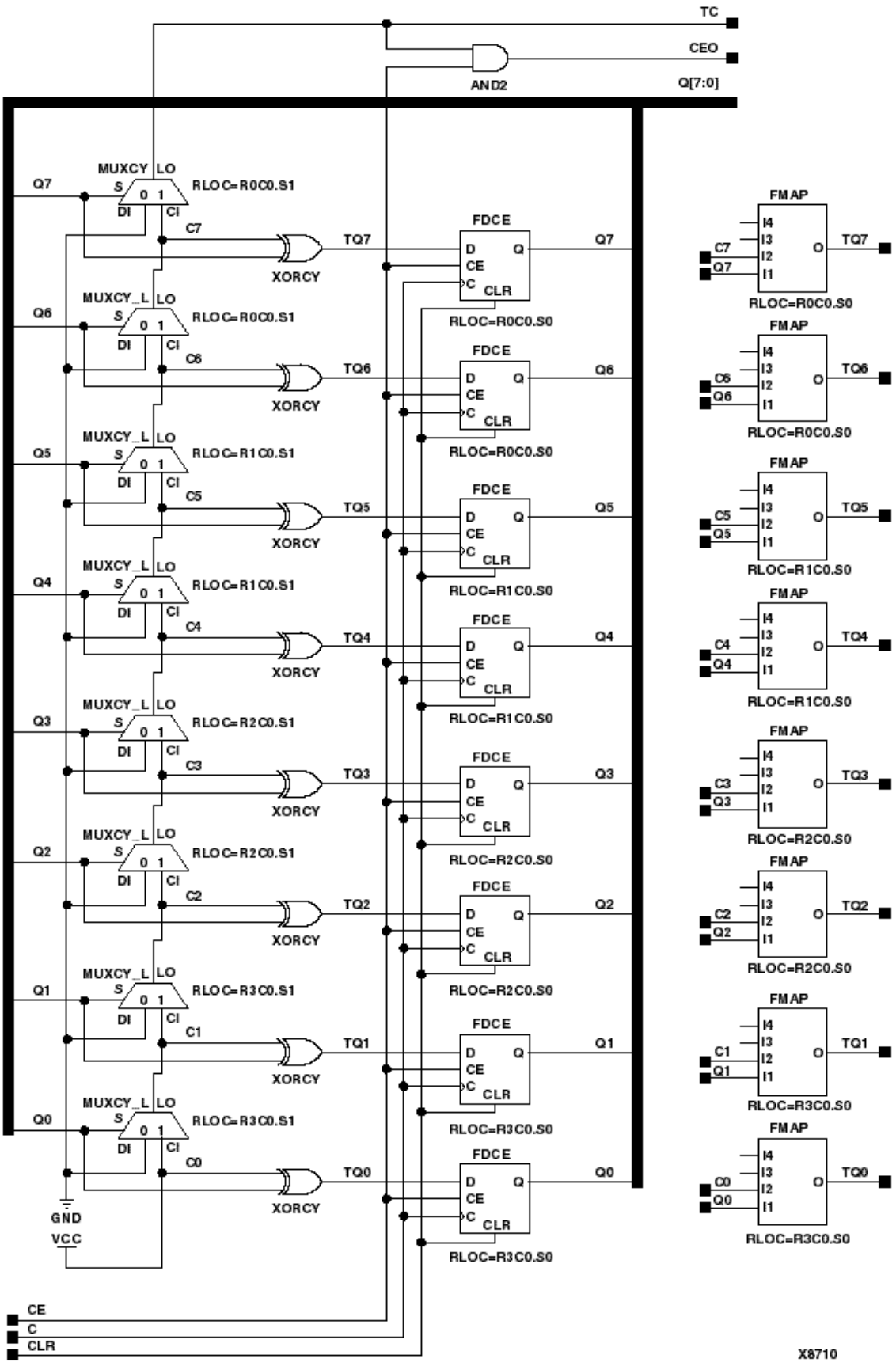


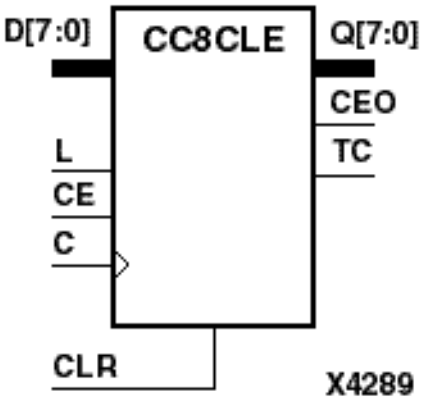
Figure 4-20CC8CE Implementation Virtex

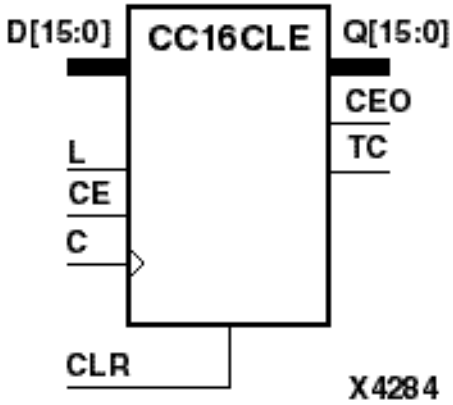

TC
CEO
Q[7:0]
AND2
MUXCY_L
LO
S
0 1
DI
CI
RLOC=R0C0.S1
RLOC=R1C0.S1
RLOC=R2C0.S1
RLOC=R3C0.S1
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
C7
C6
C5
C4
C3
C2
C1
C0
XORCY
TQ7
TQ6
TQ5
TQ4
TQ3
TQ2
TQ1
TQ0
FDCE
D
Q
CE
C
CLR
RLOC=R0C0.S0
RLOC=R1C0.S0
RLOC=R2C0.S0
RLOC=R3C0.S0
FMAP
I4
I3
I2
I1
O
GND
VCC
CE
C
CLR
X8710

CC8CLE, CC16CLE

8-, 16-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	Macro	N/A	Macro	Macro	Macro





CC8CLE and CC16CLE are, respectively, 8- and 16-bit (stage), synchronously loadable, asynchronously clearable, cascadable binary counter. These counters are implemented using carry logic with relative location constraints to ensure efficient placement of logic.

The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the

Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Larger counters are created by connecting the count enable out (CEO) output of the first stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE\text{-}TC})$, where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input; use the TC output if it does not.

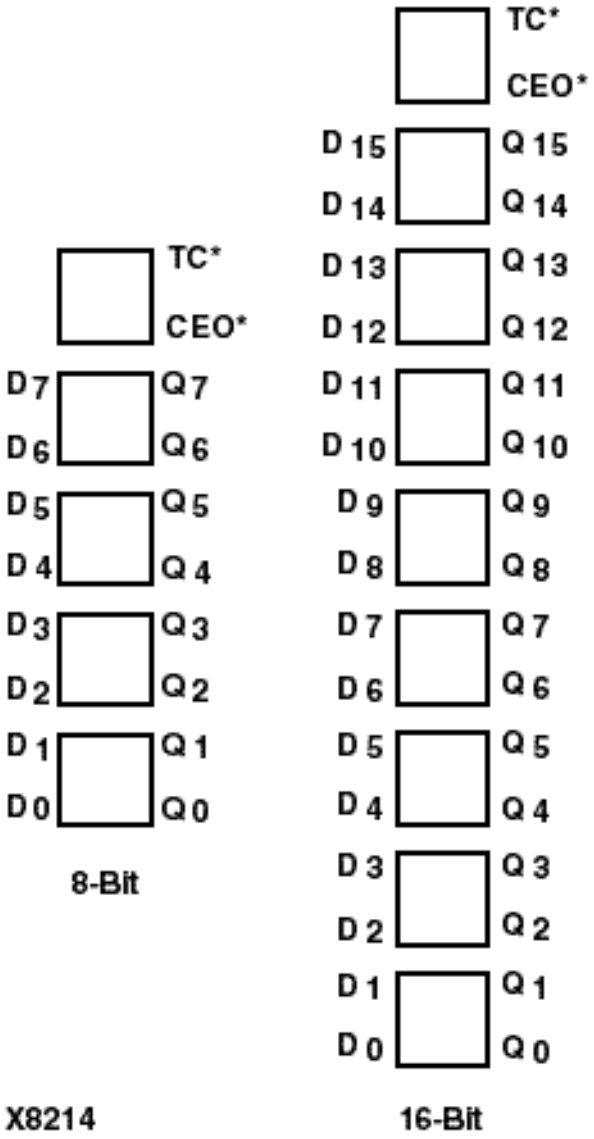
The counter is asynchronously cleared, with Low output, when power is applied. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs					**Outputs**		
CLR	**L**	**CE**	**C**	**Dz – D0**	**Qz – Q0**	**TC**	**CEO**
1	X	X	X	X	0	0	0
0	1	X	↑	Dn	dn	TC	CEO
0	0	0	X	X	No Chg	No Chg	0
0	0	1	↑	X	Inc	TC	CEO

z = 7 for CC8CLE; z = 15 for CC16CLE
dn = state of referenced input (Dn) one setup time prior to active clock transition
TC = Qz•Q(z-1)•Q(z-2)•...•Q0
CEO = TC•CE

Topology for XC4000 and Spartans

This is the CC8CLE (8-bit) and CC16CLE (16-bit) topology for XC4000 and Spartan series devices.



In the process of combining the logic that loads CEO and TC, the place and route software might map the logic that generates CEO and TC to different function generators. If this mapping occurs, the CEO and TC logic cannot be placed in the uppermost CLB as indicated in the illustration.

Topology for XC5200

This is the CC8CLE (8-bit) and CC16CLE (16-bit) topology for XC5200 devices.

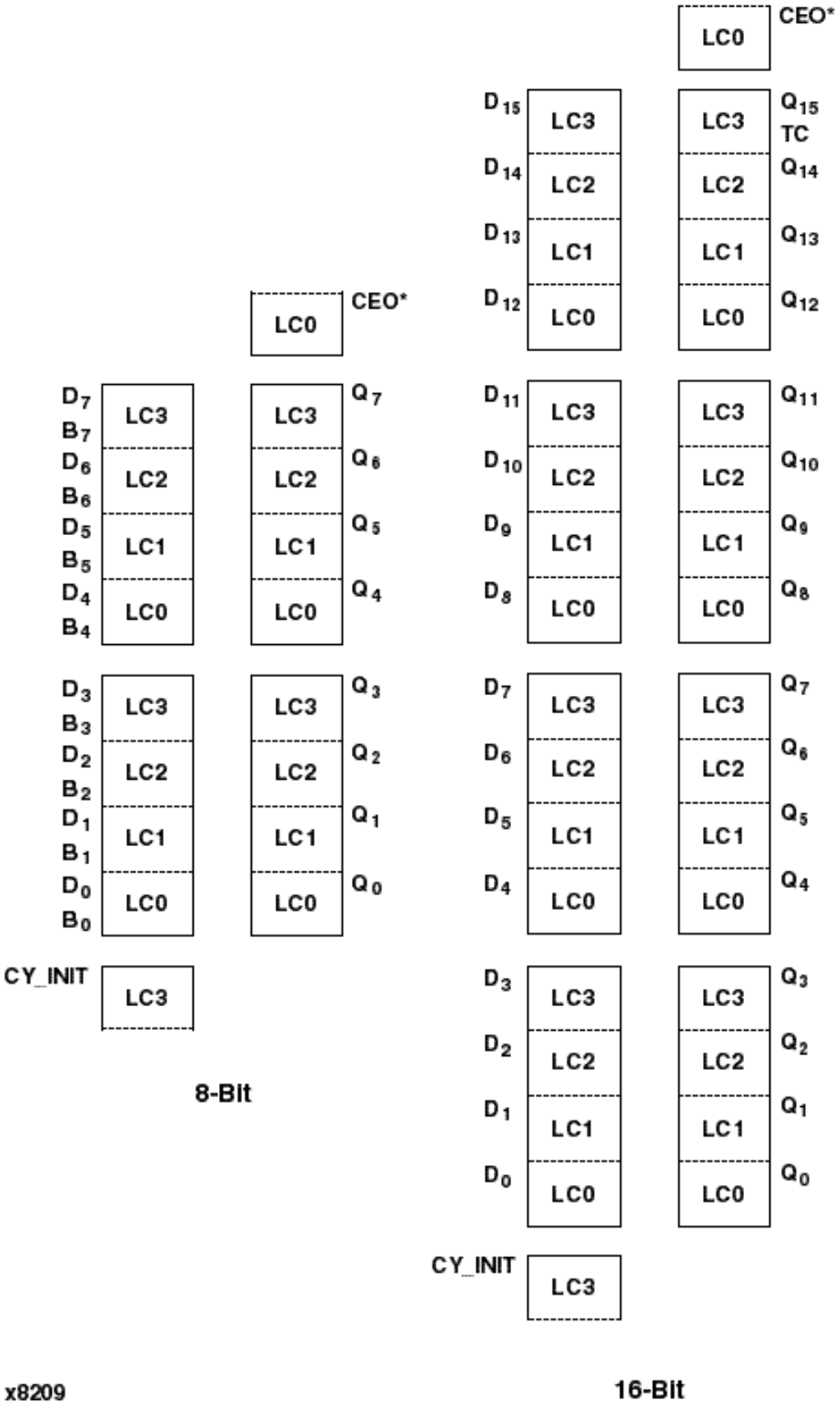

LC0
CEO*
D15
LC3
LC3
Q15
TC
D14
LC2
LC2
Q14
D13
LC1
LC1
Q13
D12
LC0
LC0
Q12
LC0
CEO*
D7
B7
LC3
LC3
Q7
D6
B6
LC2
LC2
Q6
D5
B5
LC1
LC1
Q5
D4
B4
LC0
LC0
Q4
D11
LC3
LC3
Q11
D10
LC2
LC2
Q10
D9
LC1
LC1
Q9
D8
LC0
LC0
Q8
D3
B3
LC3
LC3
Q3
D2
B2
LC2
LC2
Q2
D1
B1
LC1
LC1
Q1
D0
B0
LC0
LC0
Q0
D7
LC3
LC3
Q7
D6
LC2
LC2
Q6
D5
LC1
LC1
Q5
D4
LC0
LC0
Q4
CY_INIT
LC3
D3
LC3
LC3
Q3
D2
LC2
LC2
Q2
D1
LC1
LC1
Q1
D0
LC0
LC0
Q0
CY_INIT
LC3
8-Bit
16-Bit
x8209

Figure 4-21CC8CLE Implementation XC4000, Spartans

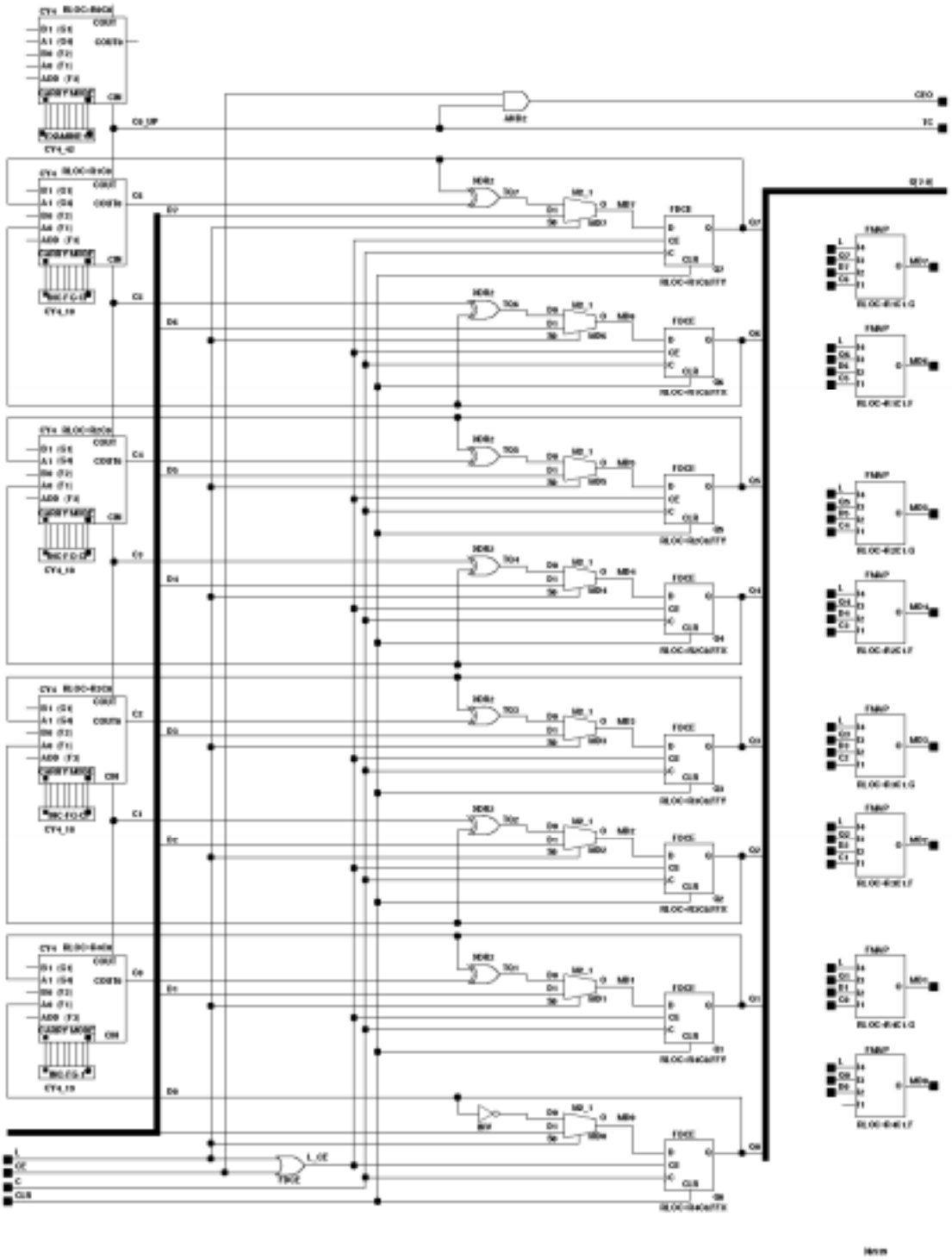


Figure 4-22CC8CLE Implementation XC5200

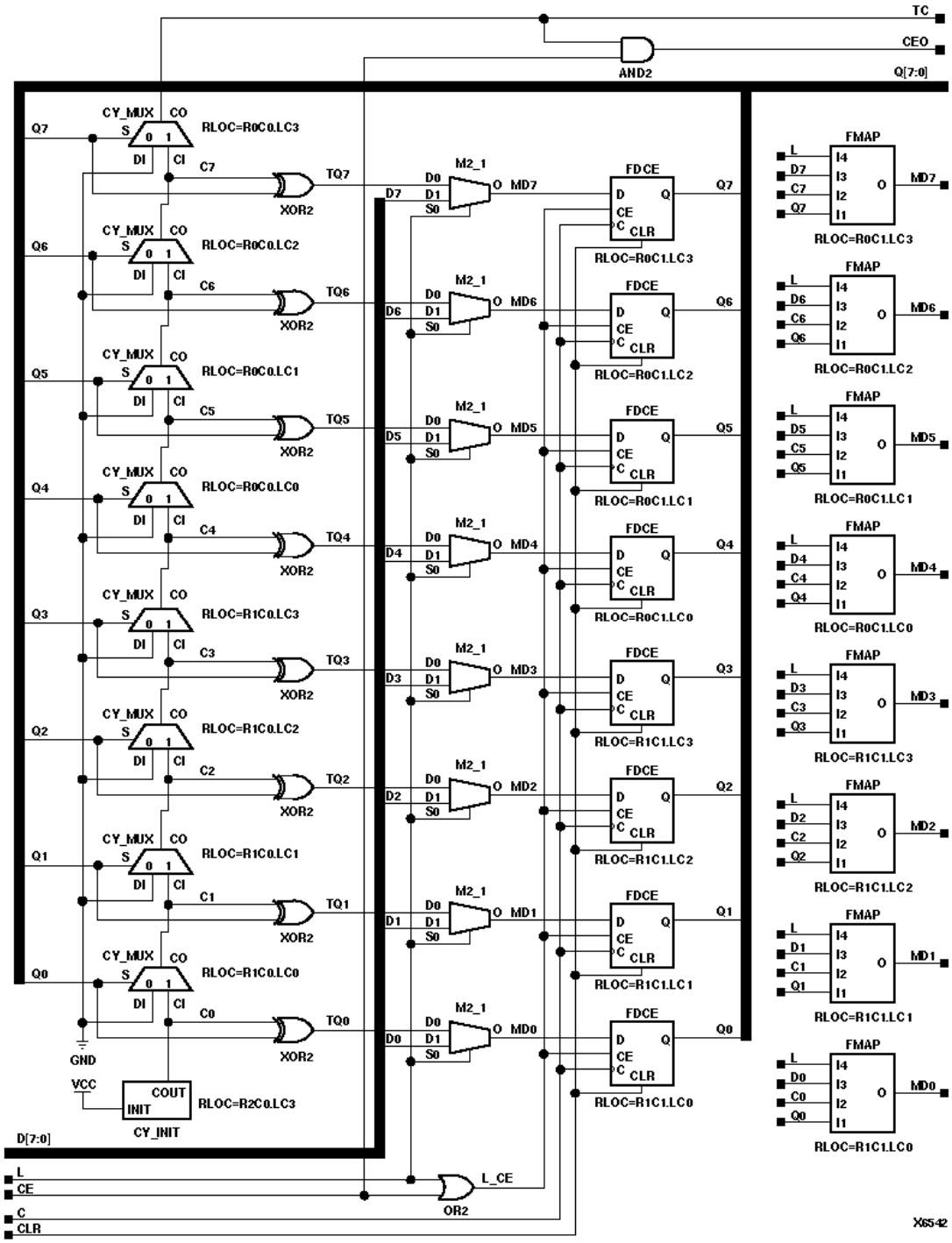
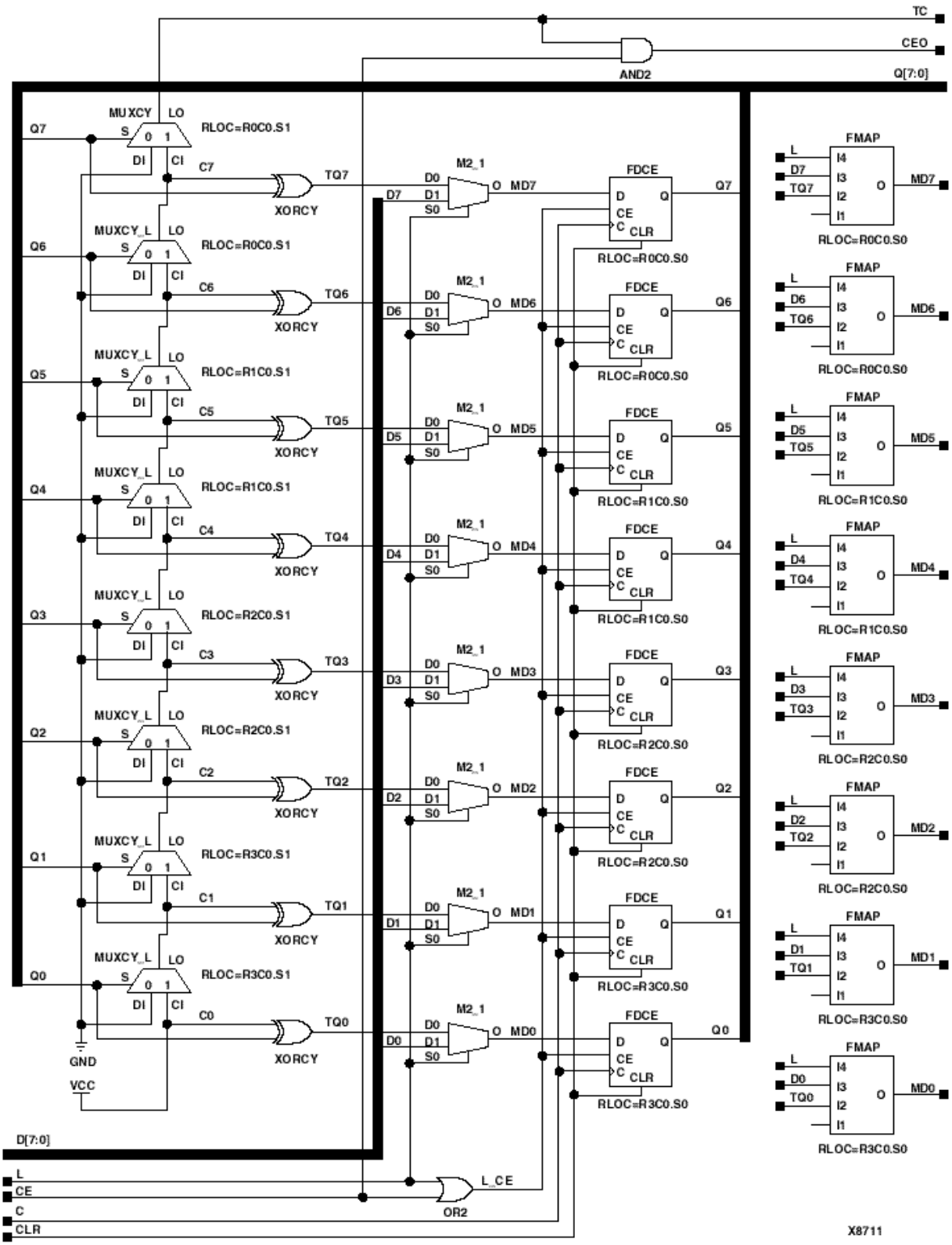


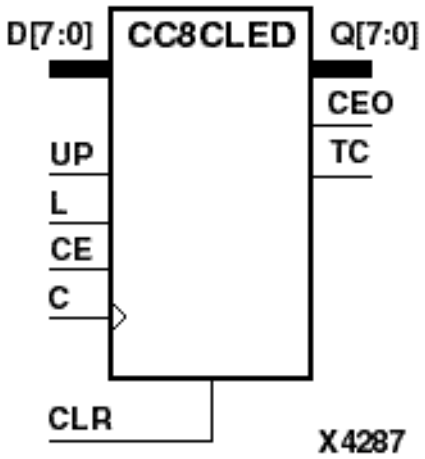
Figure 4-23CC8CLE Implementation Virtex

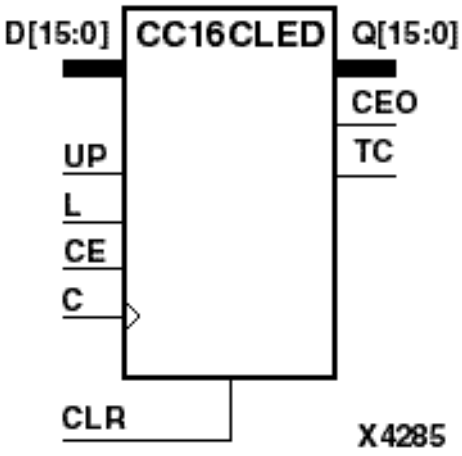


CC8CLED, CC16CLED

8-, 16-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	Macro	N/A	Macro	Macro	Macro





CC8CLED and CC16CLED are, respectively, 8- and 16-bit (stage), synchronously loadable, asynchronously clearable, cascadable, bidirectional binary counters. These counters are implemented using carry logic with relative location constraints, which assures most efficient logic placement.

The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to-High clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock

transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low. To cascade counters, the count enable out (CEO) output of each counter is connected to the CE pin of the next stage. The clock, UP, L, and CLR inputs are connected in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE\text{-}TC})$, where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input; use the TC output if it does not.

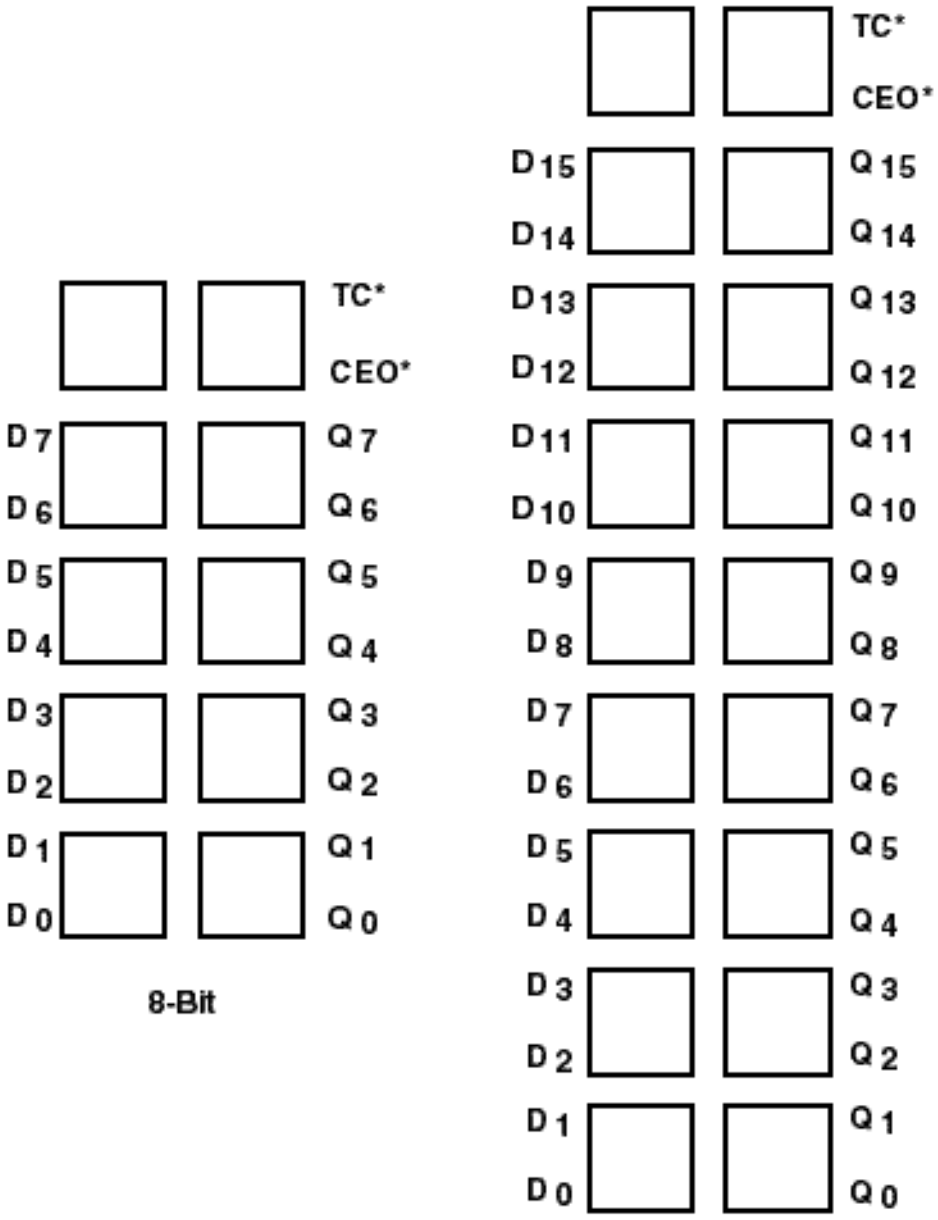
The counter is asynchronously cleared, outputs Low, when power is applied. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR (XC5200) and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs						**Outputs**		
CLR	**L**	**CE**	**C**	**UP**	**Dz – D0**	**Qz – Q0**	**TC**	**CEO**
1	X	X	X	X	X	0	0	0
0	1	X	↑	X	Dn	dn	TC	CEO
0	0	0	X	X	X	No Chg	No Chg	0
0	0	1	↑	1	X	Inc	TC	CEO
0	0	1	↑	0	X	Dec	TC	CEO

z = 7 for CC8CLED; z = 15 for CC16CLED
dn = state of referenced input (Dn) one setup time prior to active clock transition
TC = (Qz•Q(z-1)•Q(z-2)•...•Q0•UP) +
($\overline{Qz}$•$\overline{Q(z\text{-}1)}$•$\overline{Q(z\text{-}2)}$•...•$\overline{Q0}$•$\overline{UP}$)
CEO = TC•CE

Topology for XC4000 and Spartans

This is the CC8CLED (8-bit) and CC16CLED (16-bit) topology for XC4000 and Spartan series devices.



In the process of combining the logic that loads CEO and TC, the place and route software might map the logic that generates CEO and TC to different function generators. If this mapping occurs, the CEO and TC logic cannot be placed in the uppermost CLB as indicated in the illustration.

Topology for XC5200

This is the CC8CLED (8-bit) and CC16CLED (16-bit) topology for XC5200 devices.

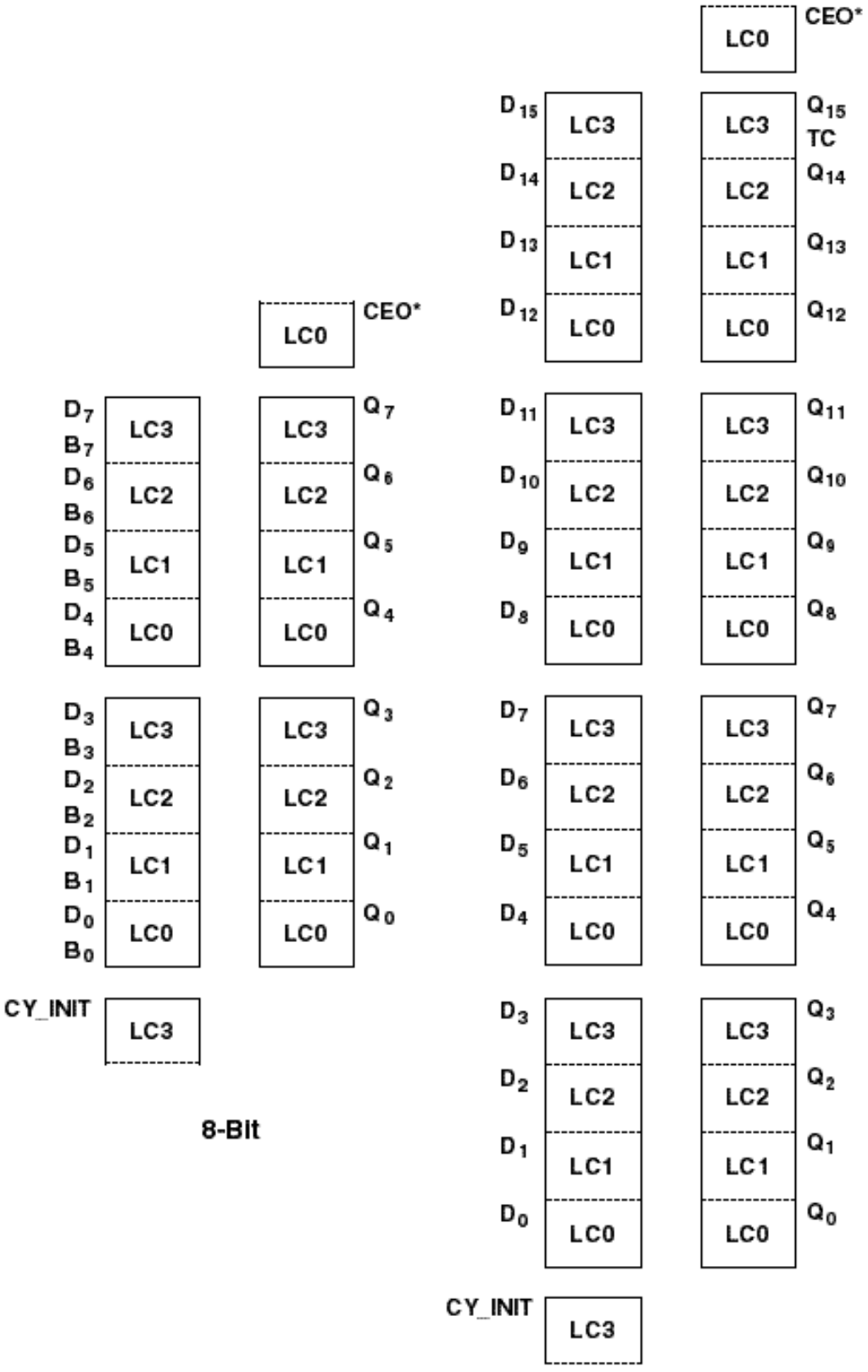

LC0
CEO*
D15
LC3
Q15
TC
D14
LC2
Q14
D13
LC1
Q13
D12
LC0
Q12
LC0
CEO*
D7
B7
LC3
Q7
D6
B6
LC2
Q6
D5
B5
LC1
Q5
D4
B4
LC0
Q4
D11
LC3
Q11
D10
LC2
Q10
D9
LC1
Q9
D8
LC0
Q8
D3
B3
LC3
Q3
D2
B2
LC2
Q2
D1
B1
LC1
Q1
D0
B0
LC0
Q0
D7
LC3
Q7
D6
LC2
Q6
D5
LC1
Q5
D4
LC0
Q4
CY_INIT
LC3
D3
LC3
Q3
D2
LC2
Q2
D1
LC1
Q1
D0
LC0
Q0
CY_INIT
LC3
8-Bit
16-Bit
x8209

Figure 4-24CC8CLED Implementation XC4000, Spartans

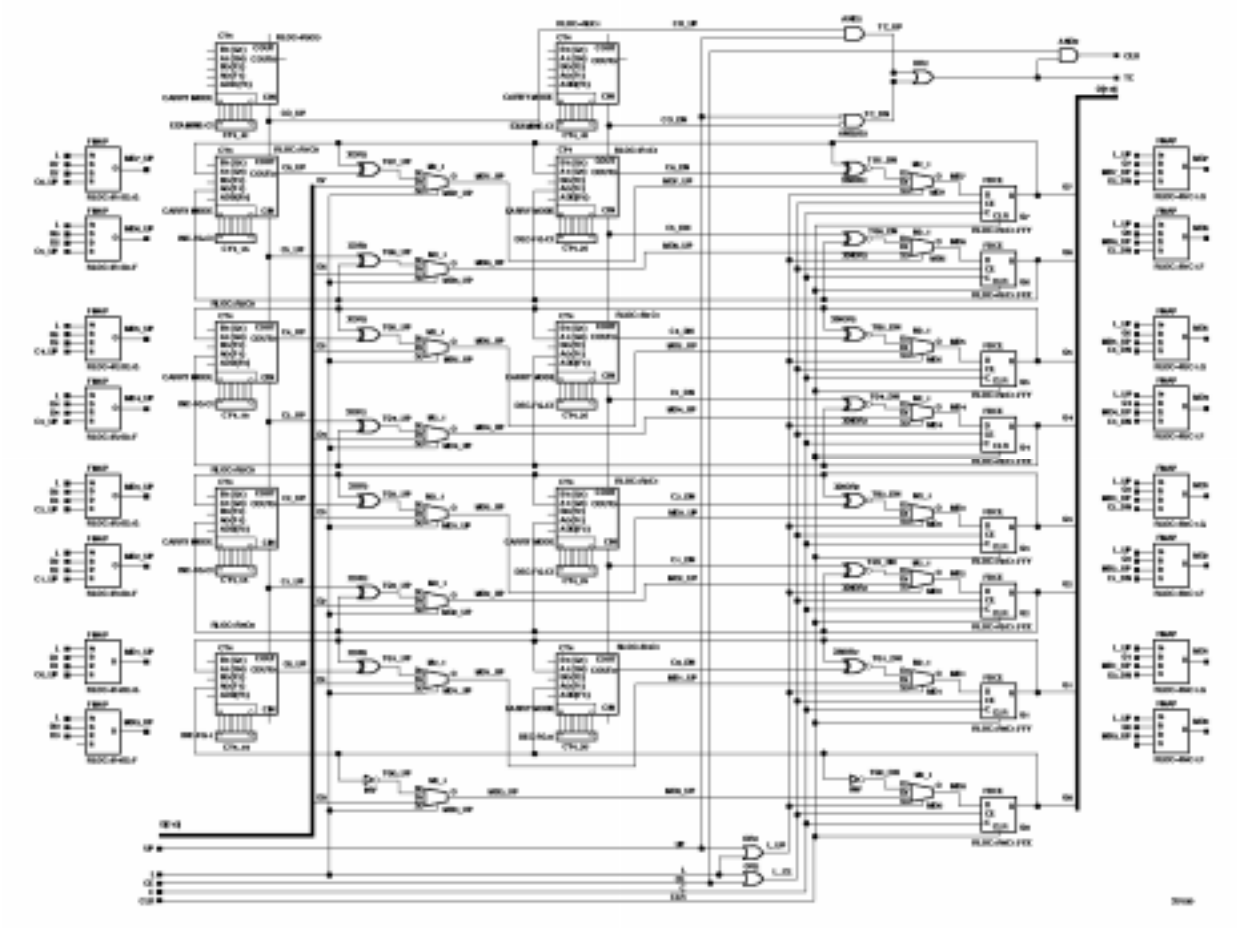


Figure 4-25CC8CLED Implementation XC5200

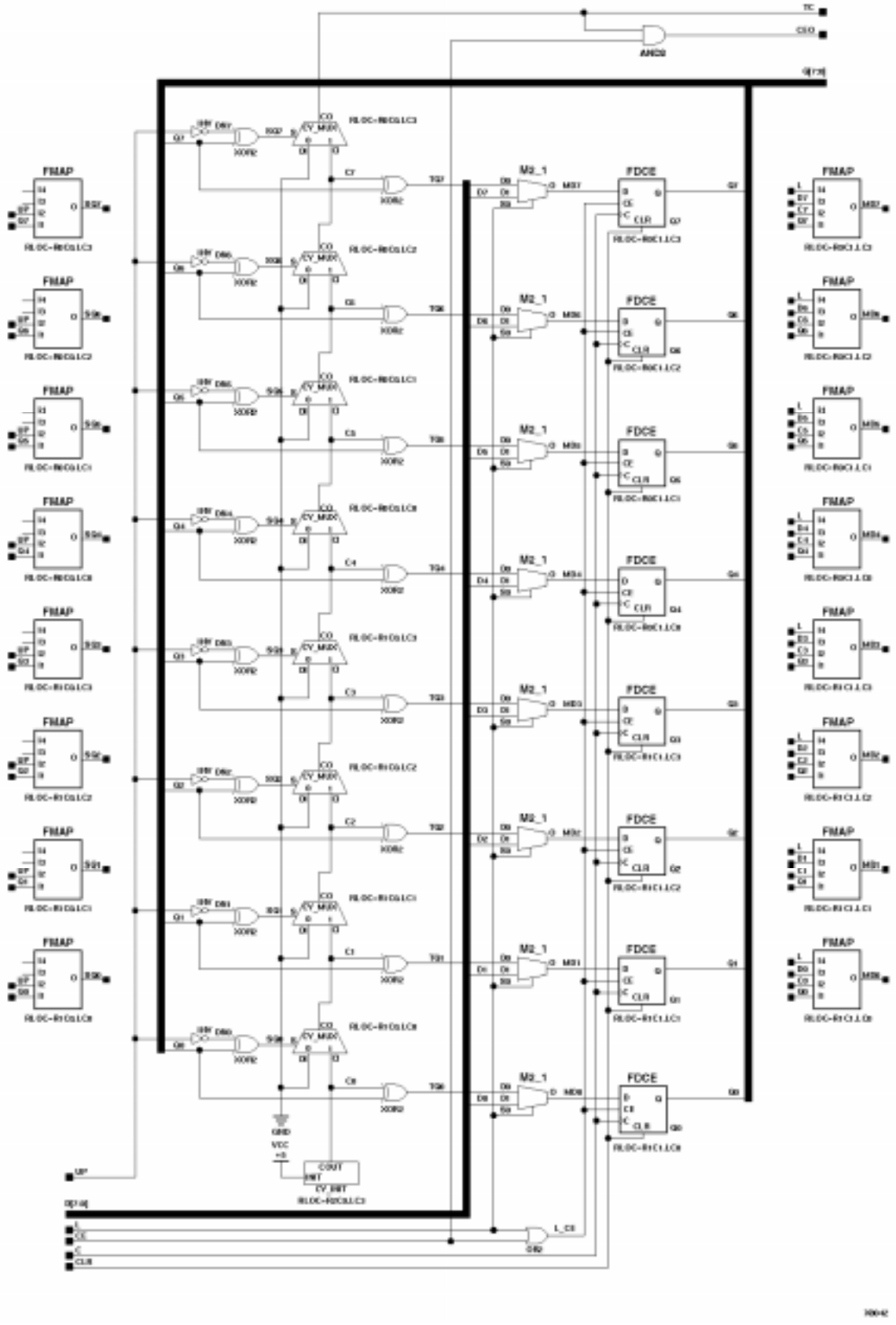
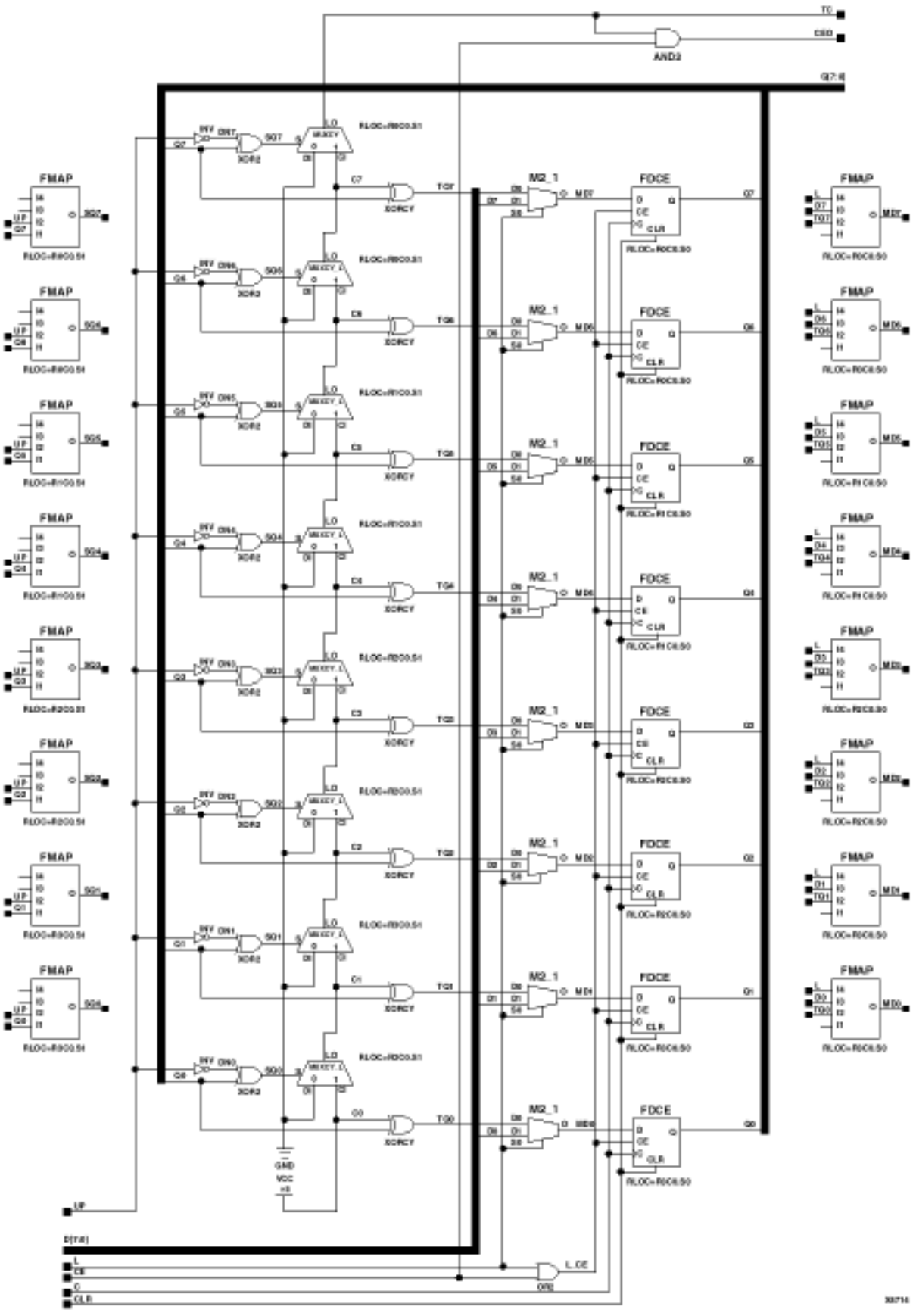

AND2
FMAP
FDCE
M2_1
GND
VCC
COUT
CV_INIT

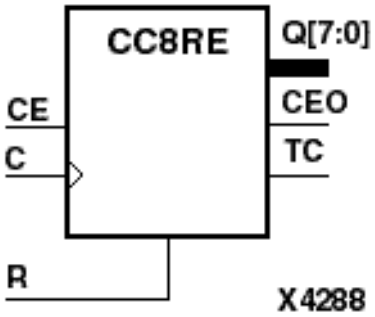
Figure 4-26CC8CLED Implementation Virtex

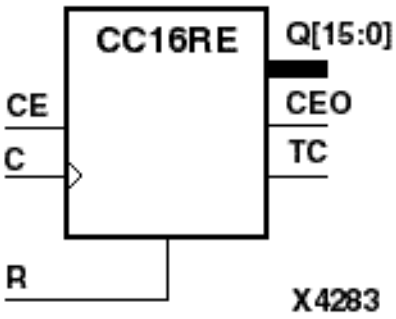

AND2
FMAP
XOR2
MUXCY
XORCY
M2_1
FDCE
GND
VCC

CC8RE, CC16RE

8-, 16-Bit Cascadable Binary Counters with Clock Enable and Synchronous Reset

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	Macro	N/A	Macro	Macro	Macro





CC8RE and CC16RE are, respectively, 8- and 16-bit (stage), synchronous, resettable, cascadable binary counters. These counters are implemented using carry logic with relative location constraints to ensure efficient placement of logic. The synchronous reset (R) is the highest priority input. When R is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero on the Low-to-High clock (C) transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs and CE are High.

Larger counters are created by connecting the CEO output of the first stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE\text{-}TC})$, where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input; use the TC output if it does

not.

The counter is asynchronously cleared, with Low outputs, when power is applied. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR (XC5200) and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs			Outputs		
R	**CE**	**C**	**Qz – Q0**	**TC**	**CEO**
1	X	↑	0	0	0
0	0	X	No Chg	No Chg	0
0	1	↑	Inc	TC	CEO

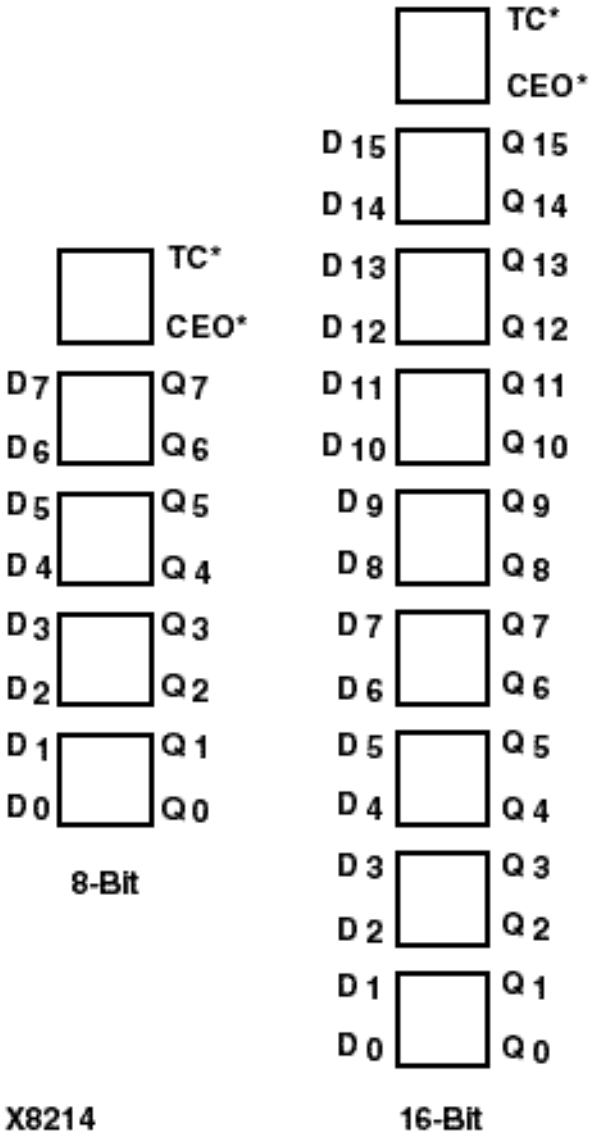
z = 7 for CC8RE; z = 15 for CC16RE

TC = Qz•Q(z-1)•Q(z-2)•...•Q0•CE

CEO = TC•CE

Topology for XC4000 and Spartans

This is the CC8RE (8-bit) and CC16RE (16-bit) topology for XC4000 and Spartan series devices.



In the process of combining the logic that loads CEO and TC, the place and route software might map the logic that generates CEO and TC to different function generators. If this mapping occurs, the CEO and TC logic cannot be placed in the uppermost CLB as indicated in the illustration.

Topology for XC5200

This is the CC8RE (8-bit) and CC16RE (16-bit) topology for XC5200 devices.

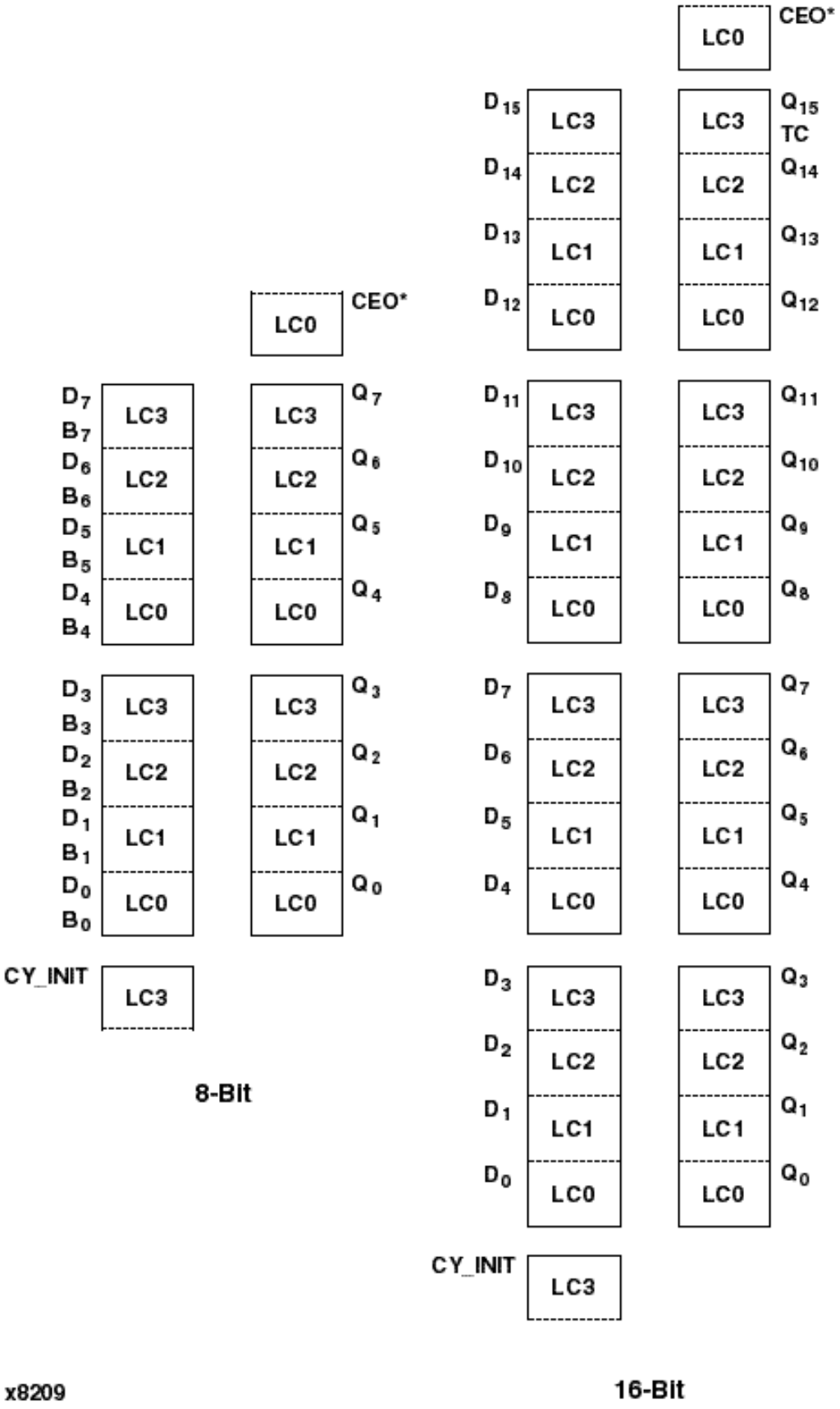

LC0
CEO*
D15
LC3
Q15
TC
D14
LC2
Q14
D13
LC1
Q13
D12
LC0
Q12
D11
D10
D9
D8
Q11
Q10
Q9
Q8
D7
B7
D6
B6
D5
B5
D4
B4
Q7
Q6
Q5
Q4
D3
B3
D2
B2
D1
B1
D0
B0
Q3
Q2
Q1
Q0
CY_INIT
8-Bit
16-Bit
x8209

Figure 4-27CC8RE Implementation XC4000, Spartans

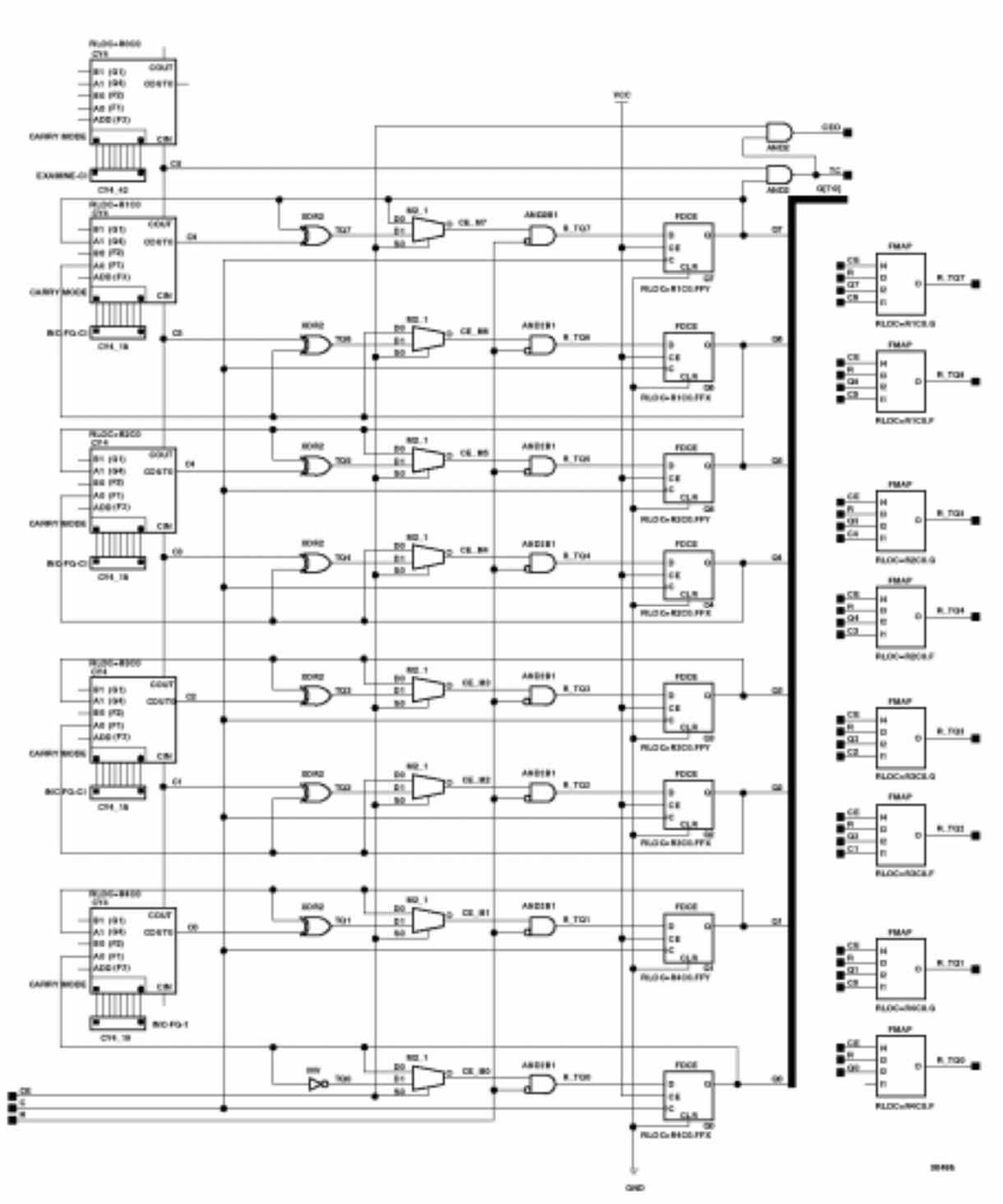


Figure 4-28CC8RE Implementation XC5200

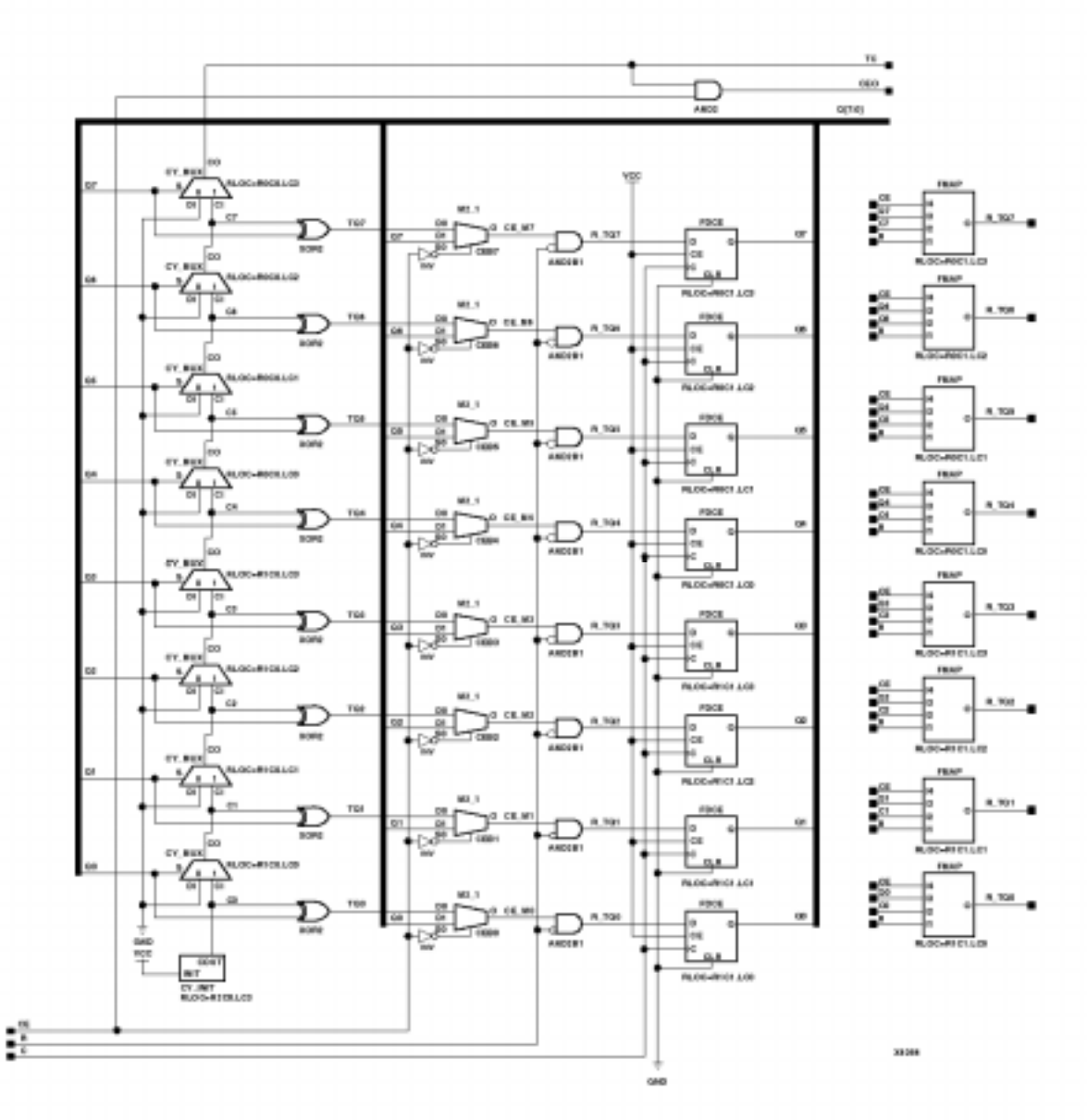
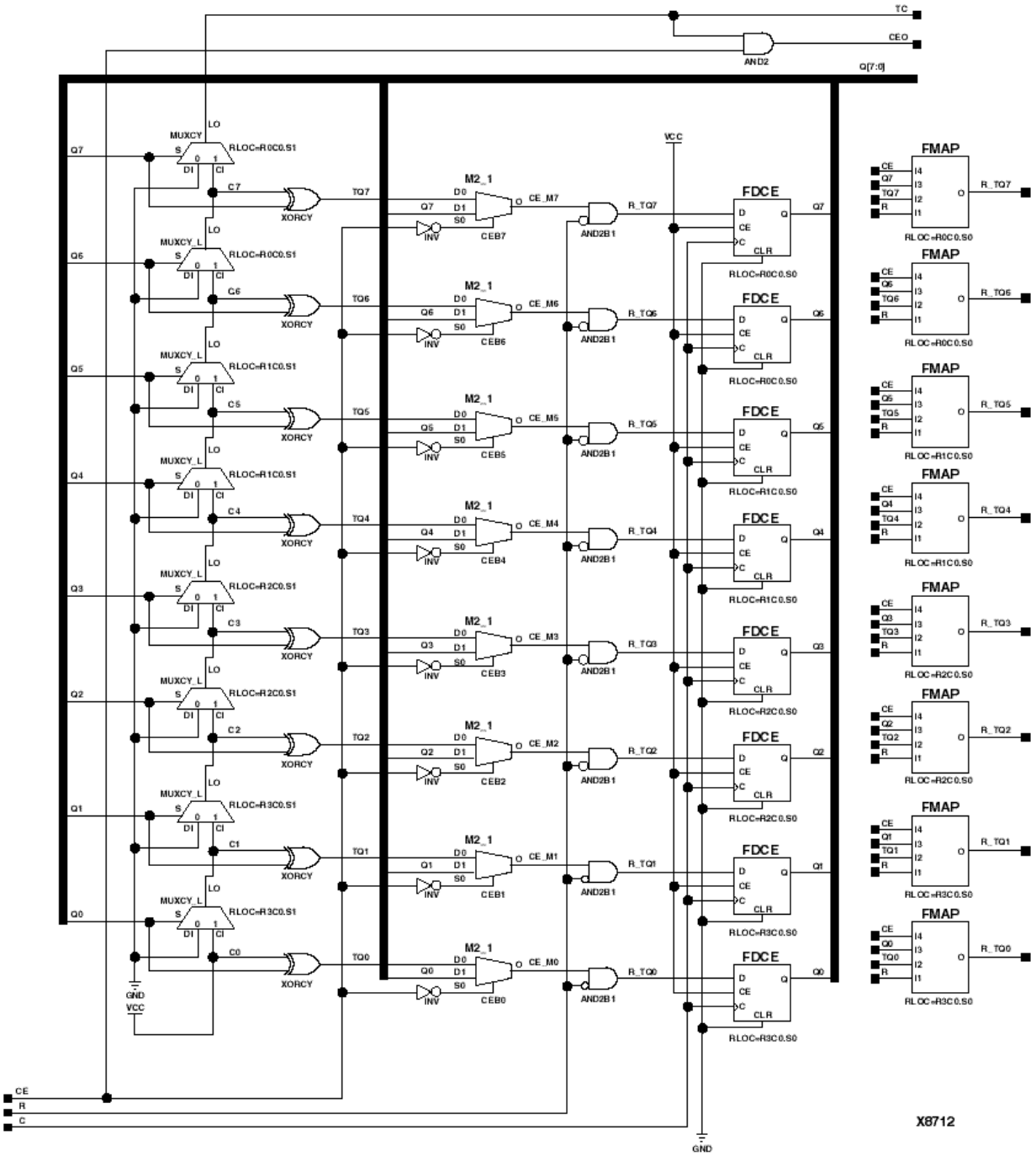


Figure 4-29CC8RE Implementation Virtex



CD4CE

4-Bit Cascadable BCD Counter with Clock Enable and Asynchronous Clear

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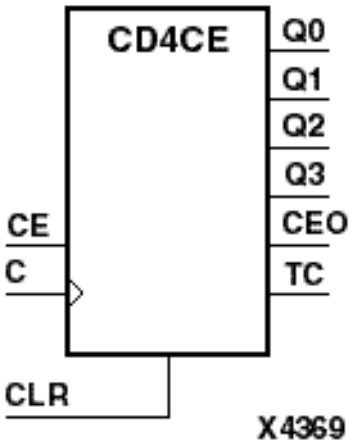
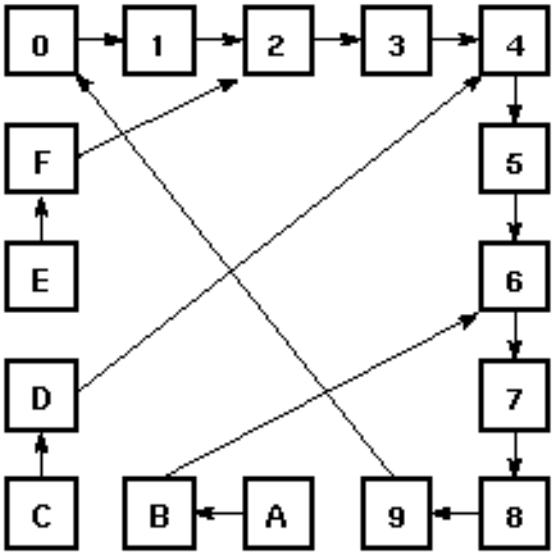
XC3000 **XC4000** **XC4000** **XC5200** **XC9000** **Spartan** **Spartan** **Virtex**

E		X				XL	
Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro



CD4CE is a 4-bit (stage), asynchronous, clearable, cascadable binary-coded-decimal (BCD) counter. The asynchronous clear input (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The Q outputs increment when clock enable (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when Q3 and Q0 are High and Q2 and Q1 are Low.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles for FPGA architectures, as shown in the following state diagram. For XC9000, the counter resets to zero or recovers within the first clock cycle.



X2355

Larger counters are created by connecting the count enable out (CEO) output of the first stage to the CE input of the next stage and connecting the CLR and clock inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE\text{-}TC})$, where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input; use the TC output if it does not.

The counter is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse to the PRLD global net. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs			Outputs					
CLR	**CE**	**C**	**Q3**	**Q2**	**Q1**	**Q0**	**TC**	**CEO**
1	X	X	0	0	0	0	0	0

0	1	↑	Inc	Inc	Inc	Inc	TC	CE O
0	0	X	No Chg	No Chg	No Chg	No Chg	TC	0
0	1	X	1	0	0	1	1	1

TC = Q3•$\overline{Q2}$•$\overline{Q1}$•Q0

CEO = TC•CE

Figure 4-30CD4CE Implementation XC3000, XC4000, XC5200, Spartans, Virtex

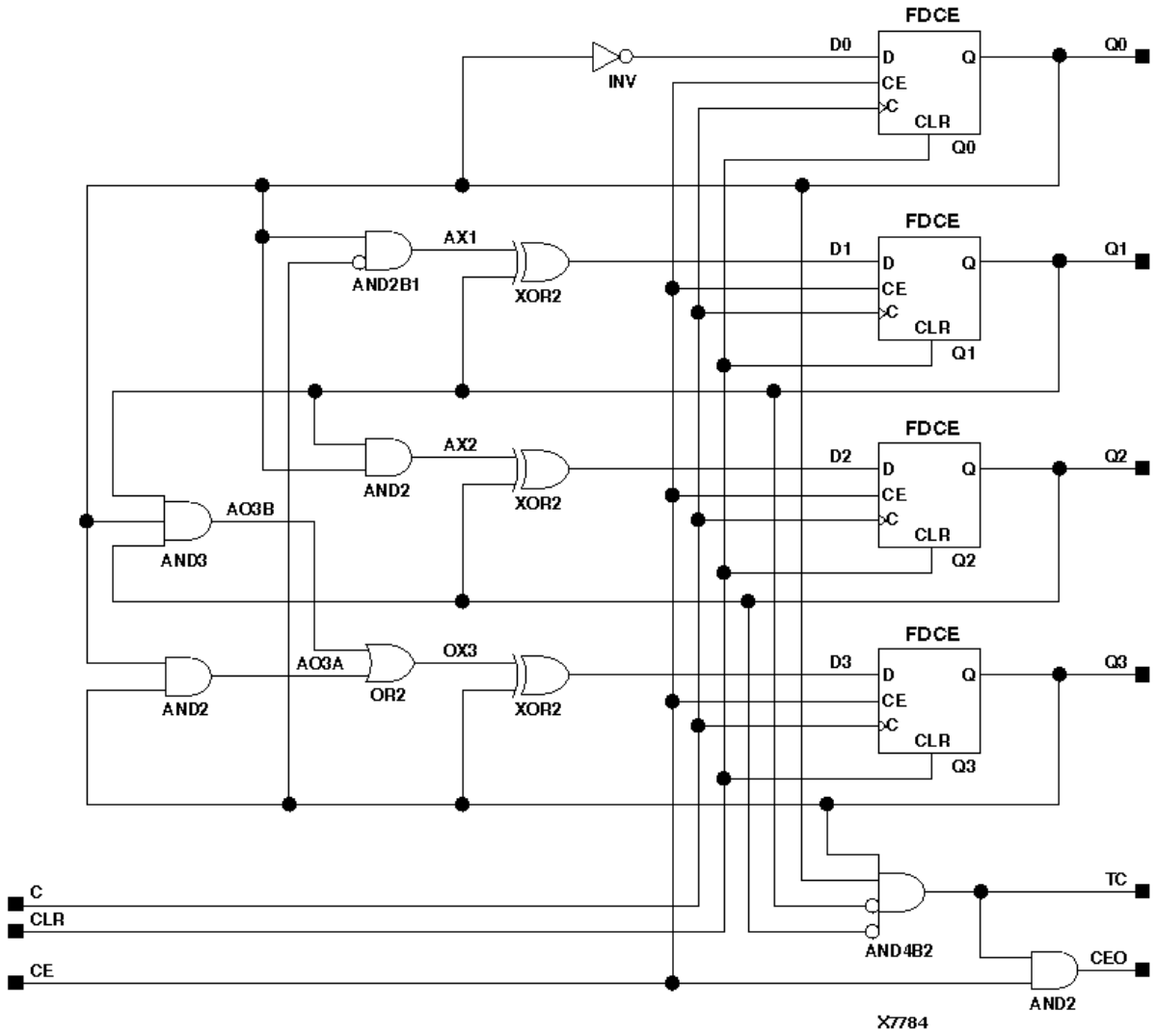
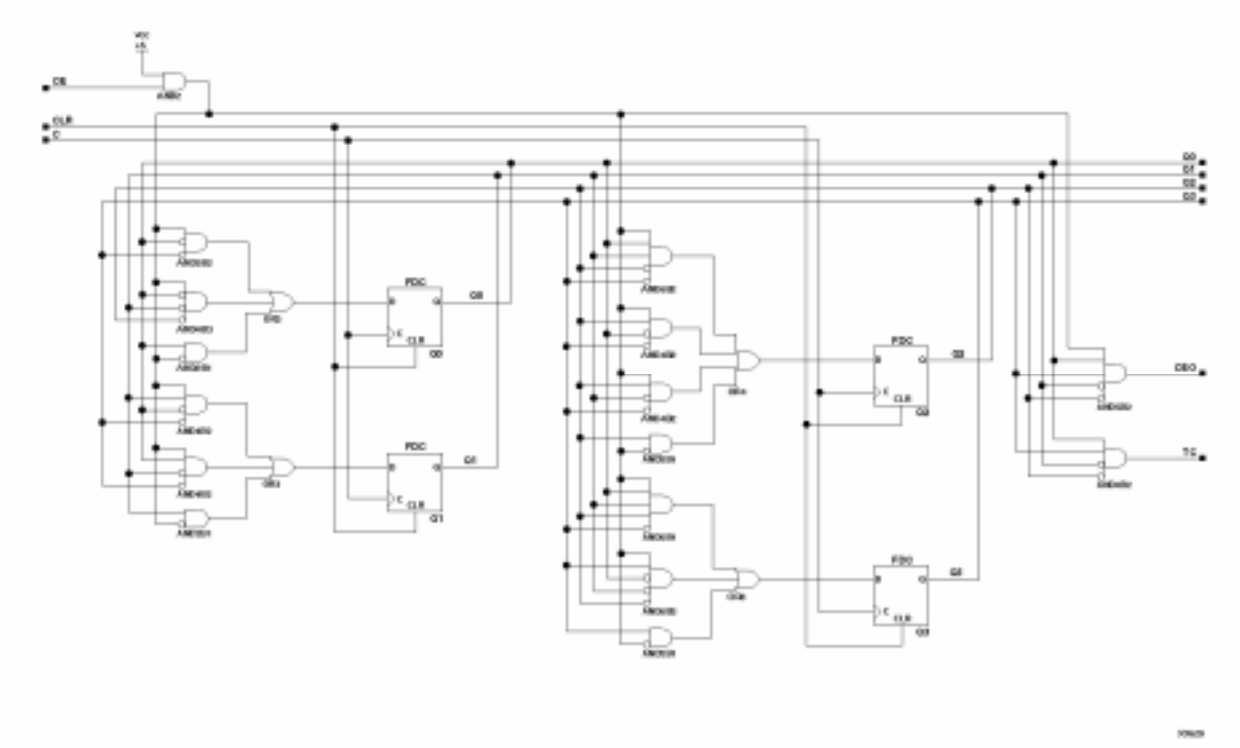


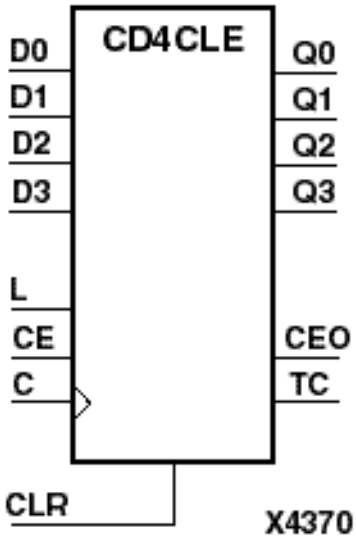
Figure 4-31CD4CE Implementation XC9000



CD4CLE

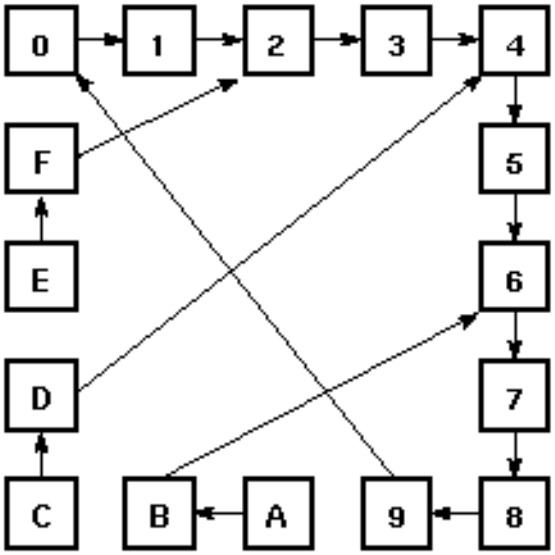
4-Bit Loadable Cascadable BCD Counter with Clock Enable and Asynchronous Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro



CD4CLE is a 4-bit (stage), synchronously loadable, asynchronously clearable, binary-coded-decimal (BCD) counter. The asynchronous clear input (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition. The Q outputs increment when clock enable input (CE) is High during the Low- to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when Q3 and Q0 are High and Q2 and Q1 are Low.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles for FPGAs, as shown in the following state diagram. For XC9000, the counter resets to zero or recovers within the first clock cycle.



Larger counters are created by connecting the count enable out (CEO) output of the first stage to the CE input of the next stage and connecting the CLR, L, and C inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE\text{-}TC})$, where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input; use the TC output if it does not.

The counter is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs					Outputs					
CLR	**L**	**CE**	**D3 – D0**	**C**	**Q3**	**Q2**	**Q1**	**Q0**	**TC**	**CEO**

1	X	X	X	X	0	0	0	0	0	0
0	1	X	D3 – D0	↑	d3	d2	d1	d0	TC	CEO
0	0	1	X	↑	Inc	Inc	Inc	Inc	TC	CEO
0	0	0	X	X	No Chg	No Chg	No Chg	No Chg	TC	0
0	0	1	X	X	1	0	0	1	1	1

d = state of referenced input one setup time prior to active clock transition

TC = Q3●$\overline{Q2}$●$\overline{Q1}$●Q0

CEO = TC●CE

Figure 4-32CD4CLE Implementation XC3000

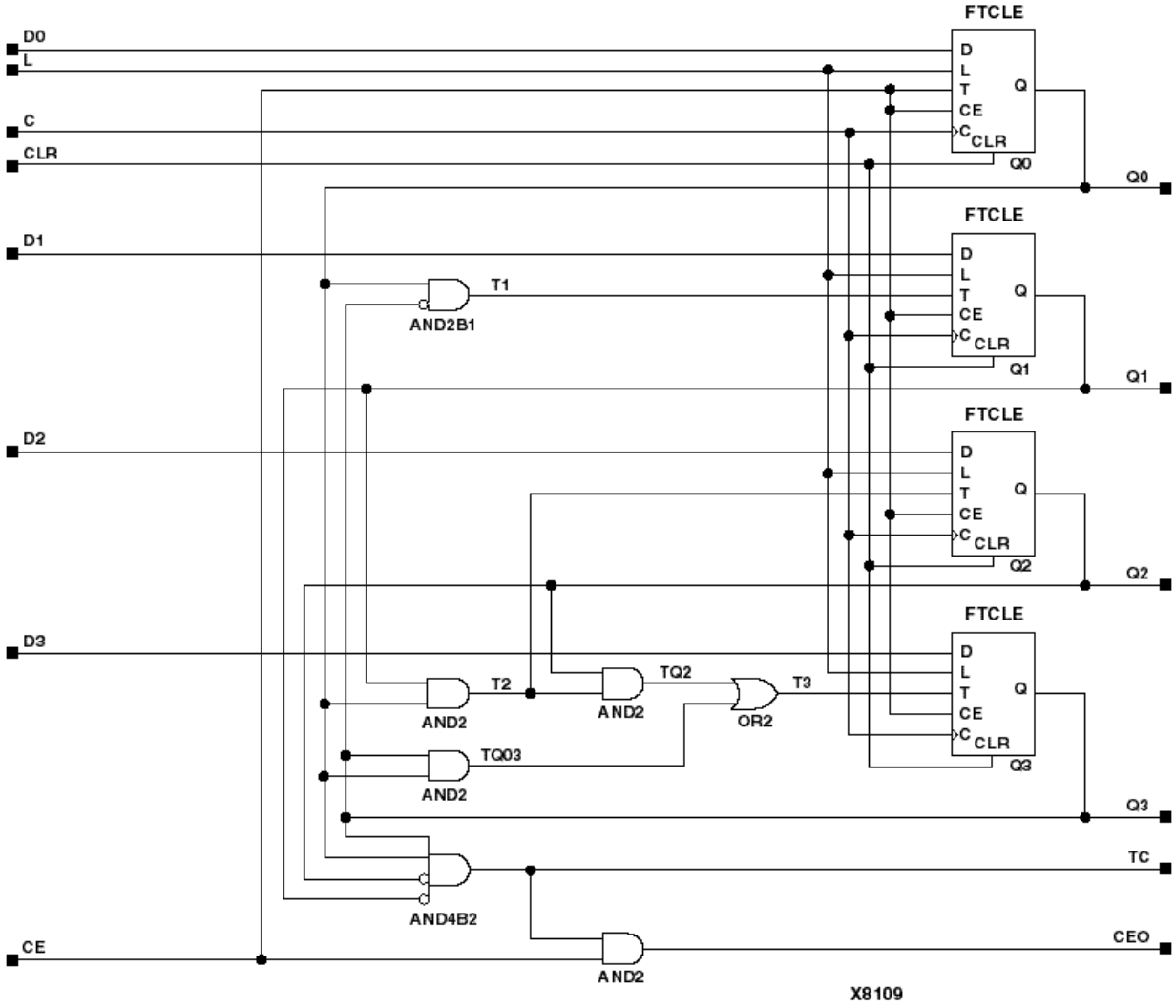


Figure 4-33CD4CLE Implementation XC4000, XC5200, Spartans, Virtex

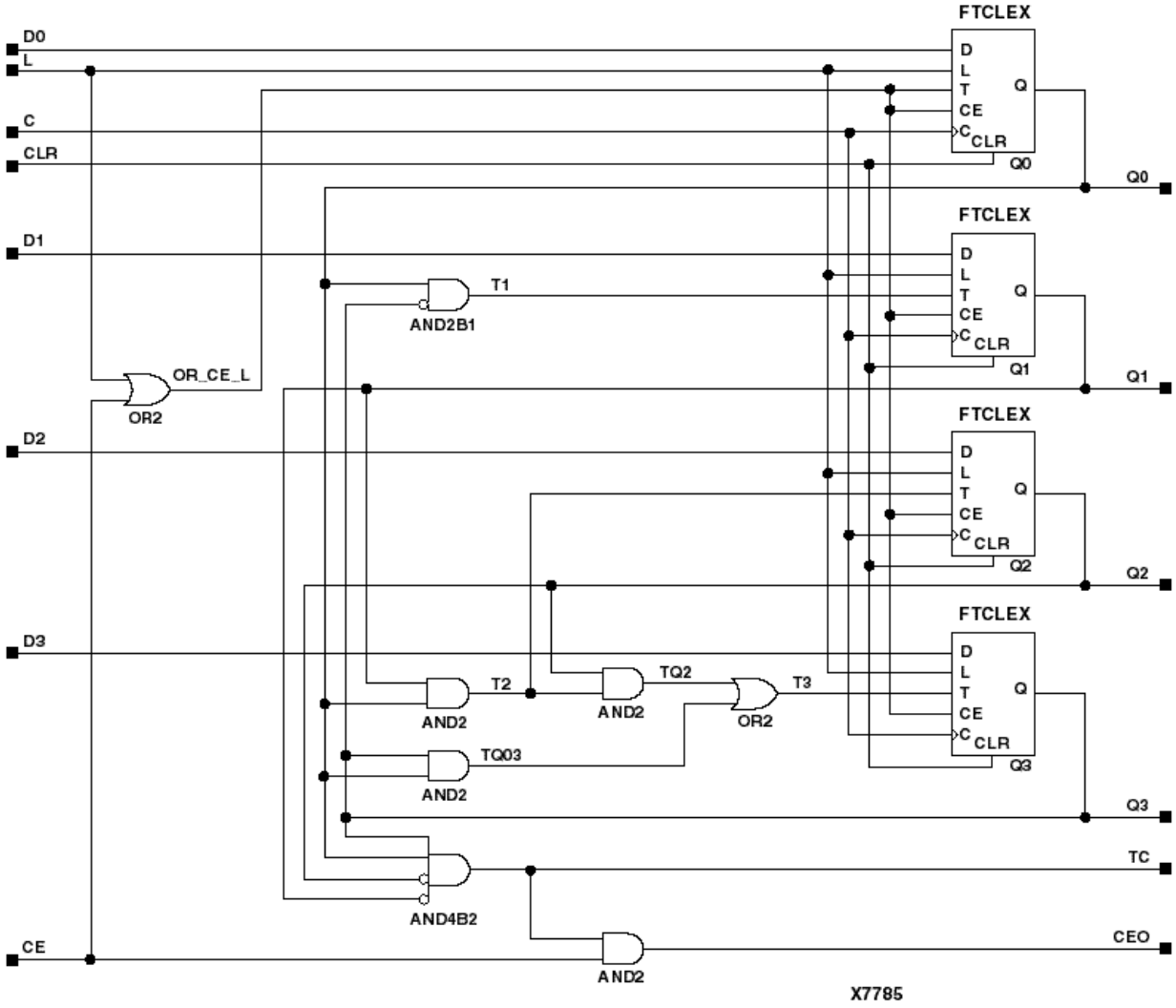
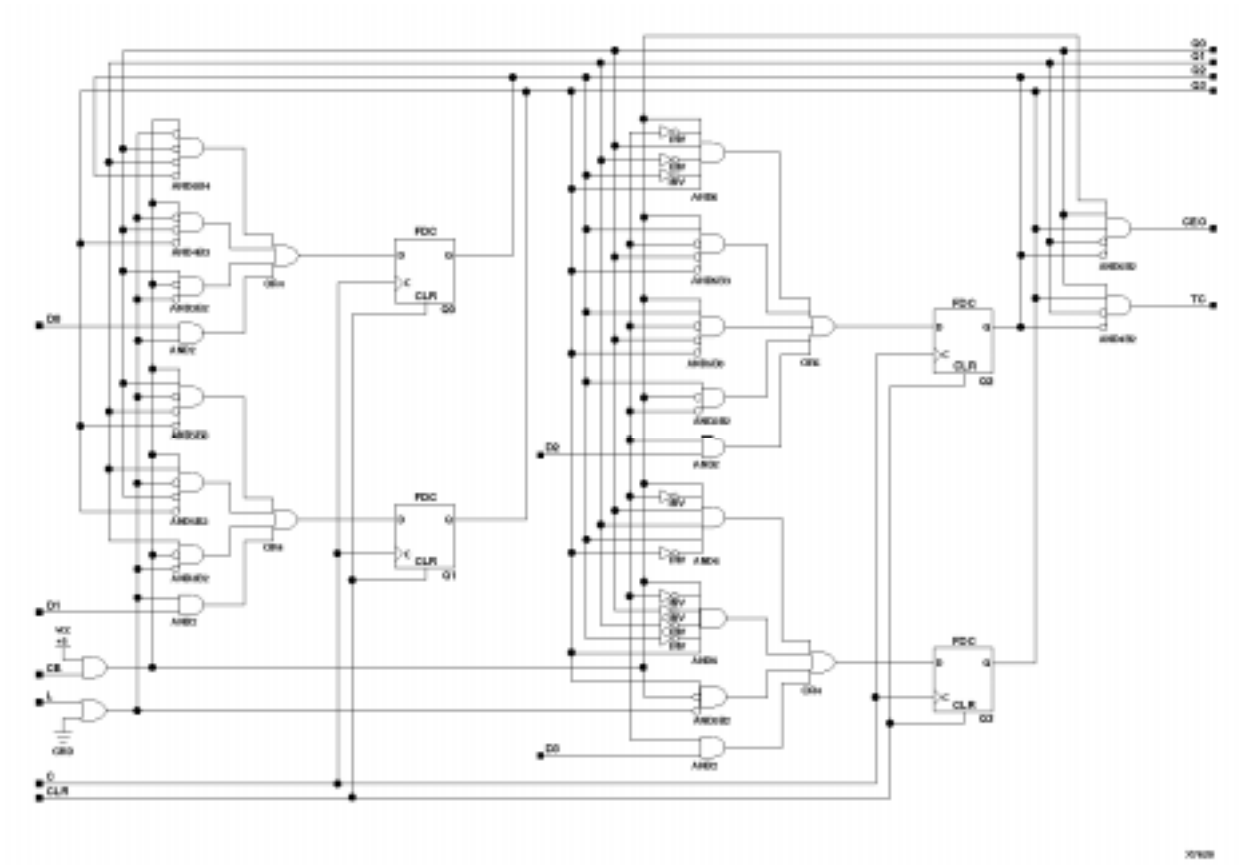


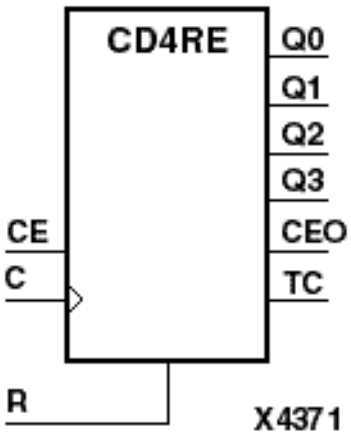
Figure 4-34CD4CLE Implementation XC9000



CD4RE

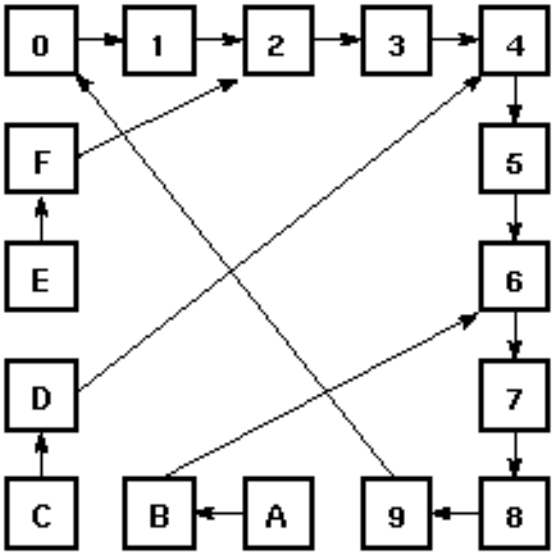
4-Bit Cascadable BCD Counter with Clock Enable and Synchronous Reset

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro



CD4RE is a 4-bit (stage), synchronous, resettable, cascadable binary-coded-decimal (BCD) counter. The synchronous reset input (R) is the highest priority input. When R is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero on the Low-to-High clock (C) transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when Q3 and Q0 are High and Q2 and Q1 are Low.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles for FPGAs, as shown in the following state diagram. For XC9000, the counter resets to zero or recovers within the first clock cycle.



X2355

Larger counters are created by connecting the count enable out (CEO) output of the first stage to the CE input of the next stage and connecting the R and clock inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE\text{-}TC})$, where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input; use the TC output if it does not.

The counter is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs			Outputs					
R	**CE**	**C**	**Q3**	**Q2**	**Q1**	**Q0**	**TC**	**CEO**
1	X	↑	0	0	0	0	0	0

0	1	↑	Inc	Inc	Inc	Inc	TC	CE O
0	0	X	No Chg	No Chg	No Chg	No Chg	TC	0
0	1	X	1	0	0	1	1	1

TC = Q3•$\overline{Q2}$•$\overline{Q1}$•Q0

CEO = TC•CE

Figure 4-35CD4RE Implementation XC3000, XC4000, XC5200, Spartans, Virtex

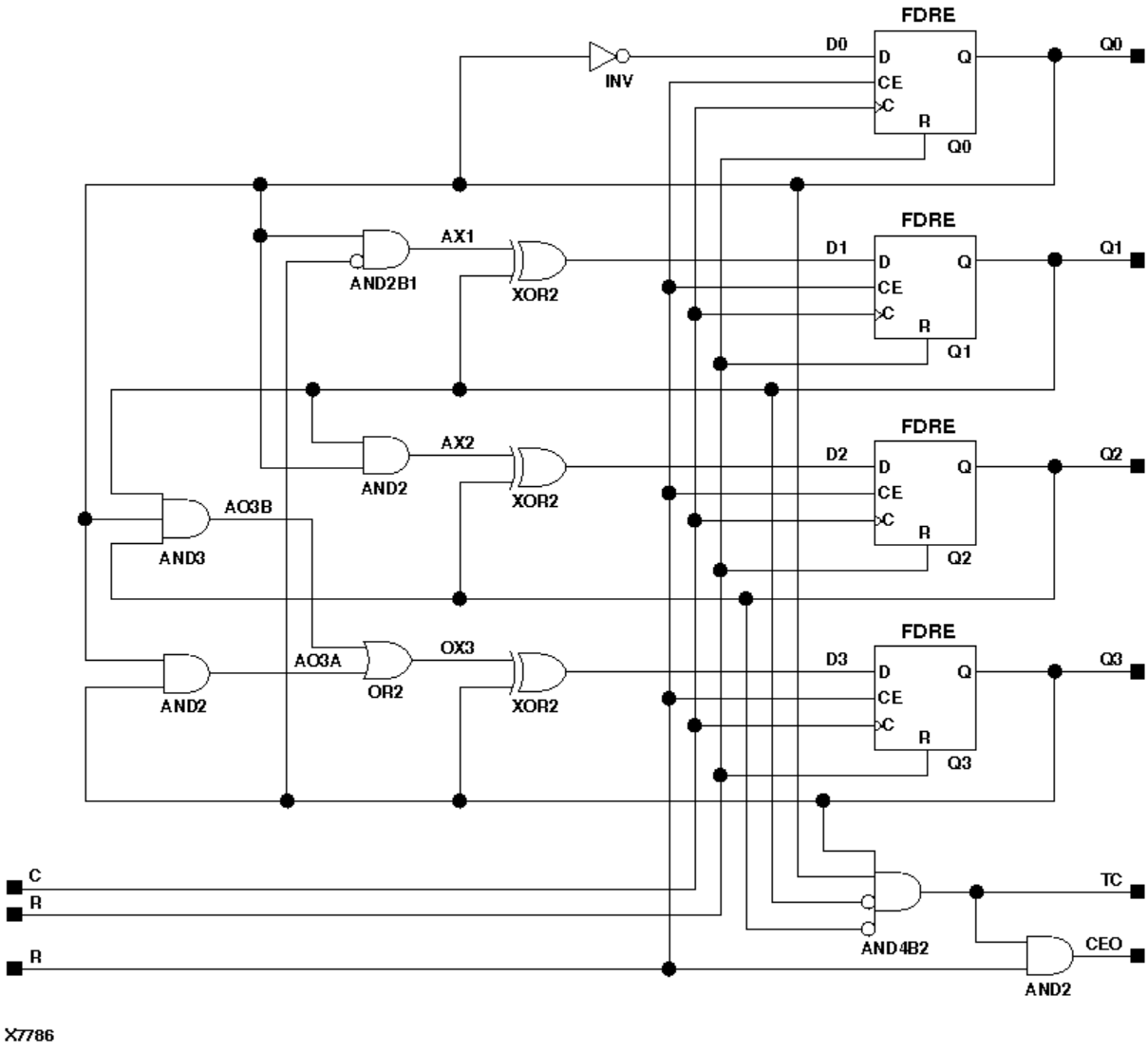
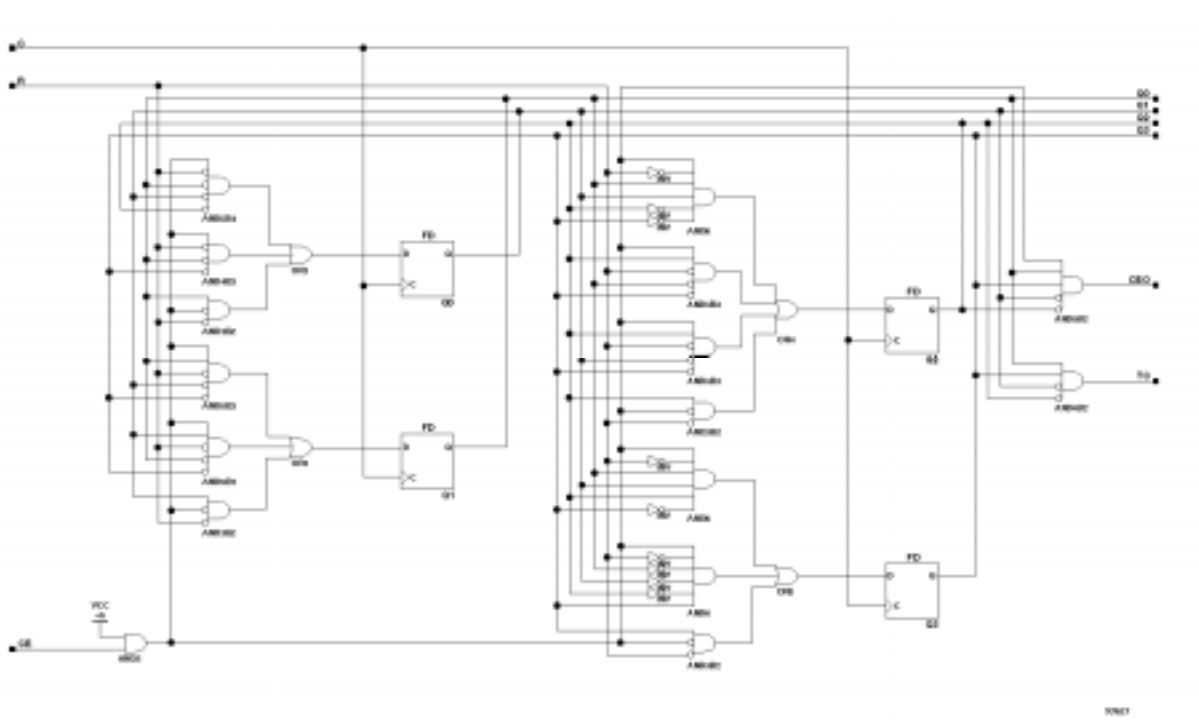


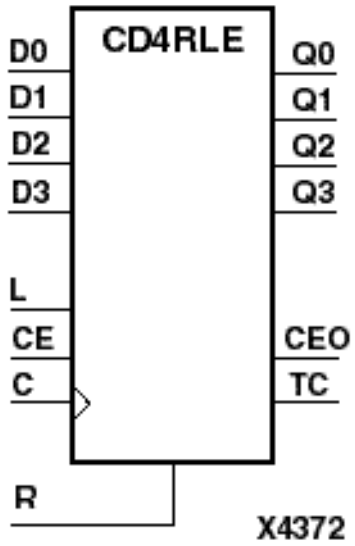
Figure 4-36CD4RE Implementation XC9000



CD4RLE

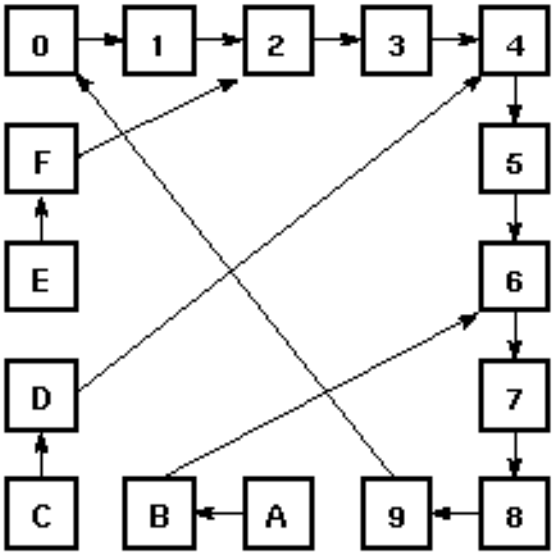
4-Bit Loadable Cascadable BCD Counter with Clock Enable and Synchronous Reset

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro



CD4RLE is a 4-bit (stage), synchronous, loadable, resettable, binary-coded-decimal (BCD) counter. The synchronous reset input (R) is the highest priority input. When R is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero on the Low-to-High clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when Q3 and Q0 are High and Q2 and Q1 are Low.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles for FPGAs, as shown in the following state diagram. For XC9000, the counter resets to zero or recovers within the first clock cycle.



X2355

Larger counters are created by connecting the count enable out (CEO) output of the first stage to the CE input of the next stage and connecting the R, L, and C inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE\text{-}TC})$, where n is the number of stages and the time $t_{CE\text{-}TC}$ is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input; use the TC output if it does not.

The counter is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs					Outputs					
R	L	CE	D3 – D0	C	Q3	Q2	Q1	Q0	TC	CEO

1	X	X	X	↑	0	0	0	0	0	0
0	1	X	D3 – D0	↑	d3	d2	d1	d0	TC	CEO
0	0	1	X	↑	Inc	Inc	Inc	Inc	TC	CEO
0	0	0	X	X	No Chg	No Chg	No Chg	No Chg	TC	0
0	0	1	X	X	1	0	0	1	1	1

d = state of referenced input one setup time prior to active clock transition

TC = Q3•$\overline{Q2}$•$\overline{Q1}$•Q0

CEO = TC•CE

Figure 4-37CD4RLE Implementation XC3000, XC4000, XC5200, Spartans, Virtex

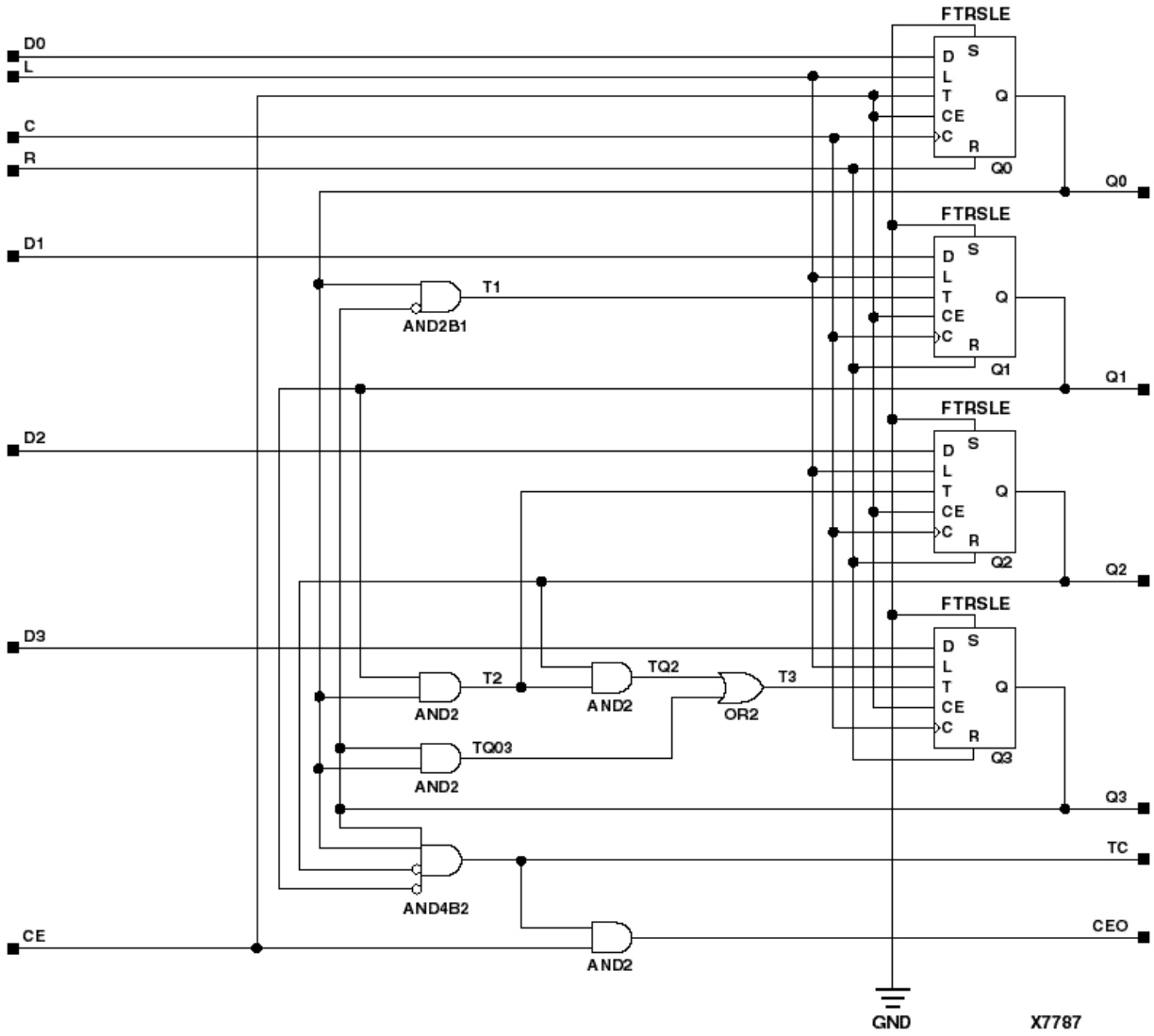
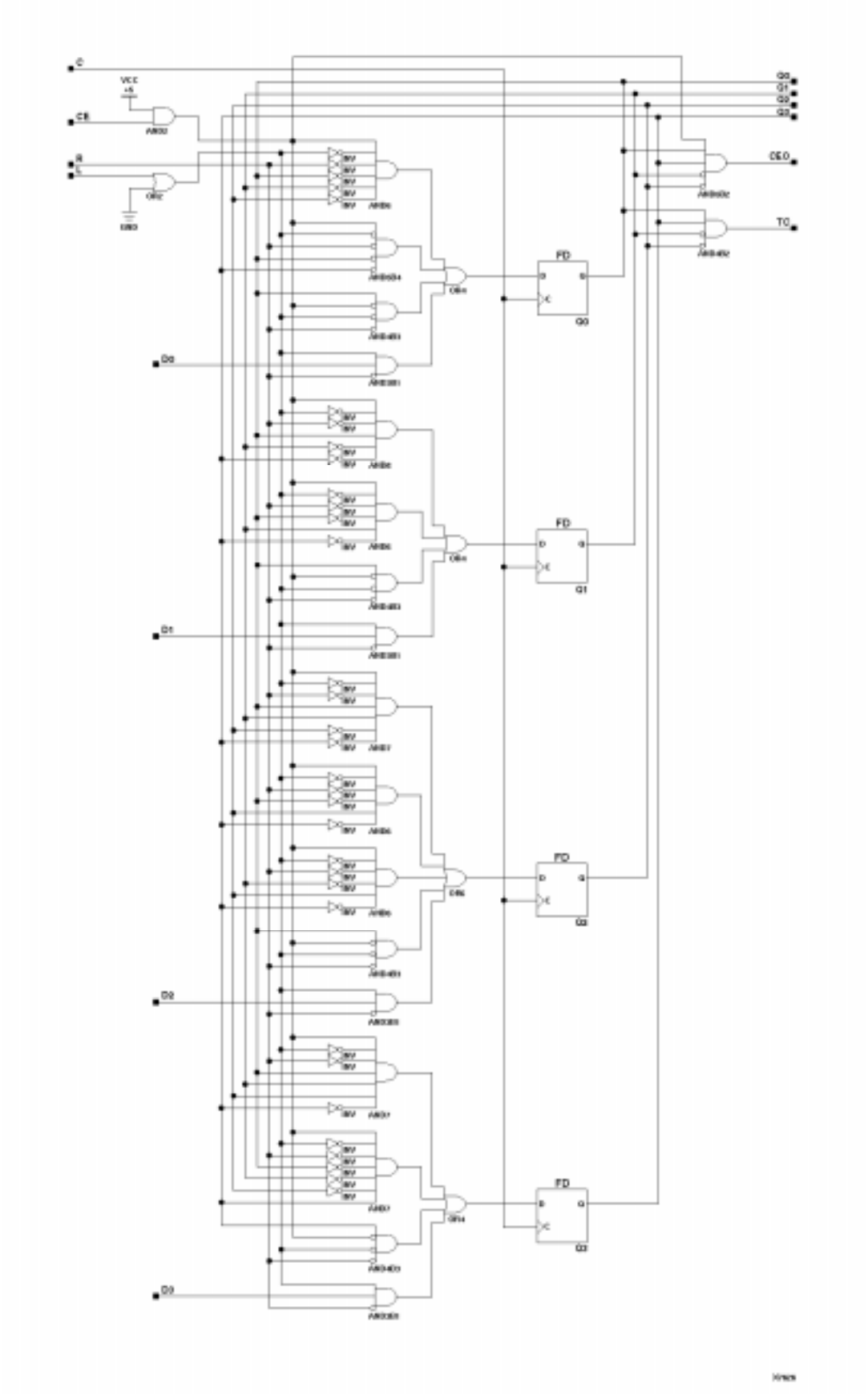


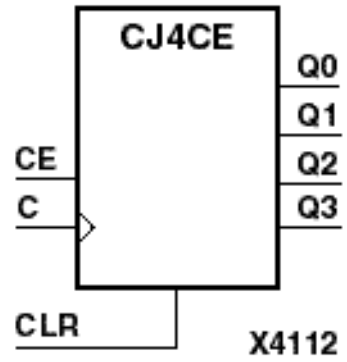
Figure 4-38CD4RLE Implementation XC9000

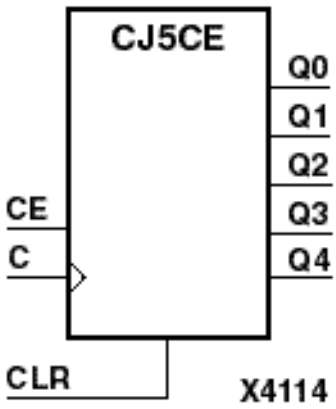

C
VCC
CE
R
GND
Q0
Q1
Q2
Q3
CEO
TC
FD
D0
D1
D2
D3

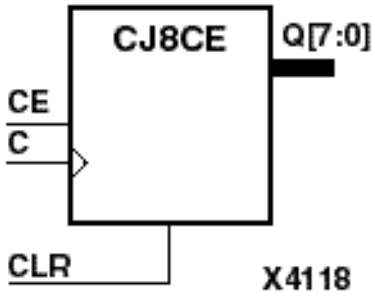
CJ4CE, CJ5CE, CJ8CE

4-, 5-, 8-Bit Johnson Counters with Clock Enable and Asynchronous Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro







CJ4CE, CJ5CE, and CJ8CE are clearable Johnson/shift counters. The asynchronous clear (CLR) input, when High, overrides all other inputs and causes the data (Q) outputs to go to logic level zero, independent of clock (C) transitions. The counter increments (shifts Q0 to Q1, Q1 to Q2,and so forth) when the clock enable input (CE) is High during the Low-to-High clock transition. Clock transitions are ignored when CE is Low.

For CJ4CE, the Q3 output is inverted and fed back to input Q0 to provide continuous counting operation. For CJ5CE, the Q4 output is inverted and fed back to input Q0. For CJ8CE, the Q7 output is inverted and fed back to input Q0.

The counter is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs			**Outputs**			
CLR	**CE**	**C**	**Q0**	**Q1**	**Q2**	**Q3**
1	X	X	0	0	0	0
0	0	X	No Chg	No Chg	No Chg	No Chg
0	1	↑	$\overline{q3}$	q0	q1	q2

q = state of referenced output one setup time prior to active clock transition

CJ4CE Truth Table

Inputs			**Outputs**				
CLR	**CE**	**C**	**Q0**	**Q1**	**Q2**	**Q3**	**Q4**
1	X	X	0	0	0	0	0
0	0	X	No Chg	No Chg	No Chg	No Chg	No Chg
0	1	↑	$\overline{q4}$	q0	q1	q2	q3

q = state of referenced output one setup time prior to active clock transition

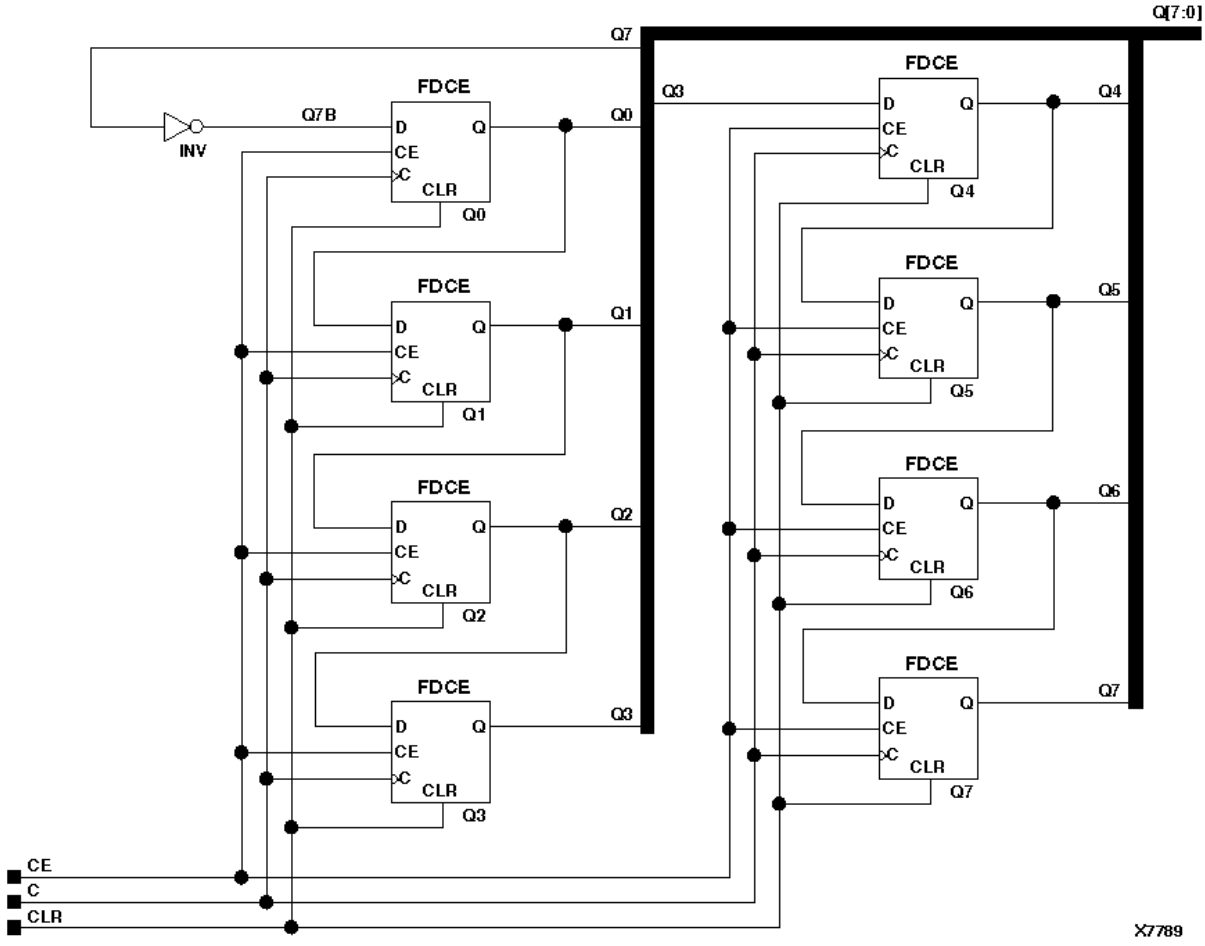
CJ5CE Truth Table

Inputs			Outputs	
CLR	**CE**	**C**	**Q0**	**Q1 – Q7**
1	X	X	0	0
0	0	X	No Chg	No Chg
0	1	↑	$\overline{q7}$	q0 – q6

q = state of referenced output one setup time prior to active clock transition

CJ8CE Truth Table

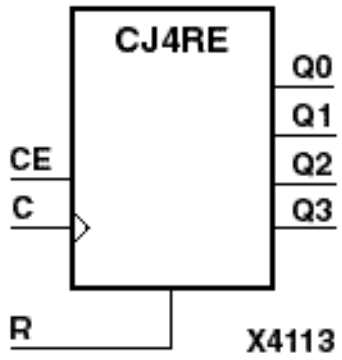
Figure 4-39CJ8CE Implementation XC3000, XC4000, XC5200, XC9000, Spartans, Virtex

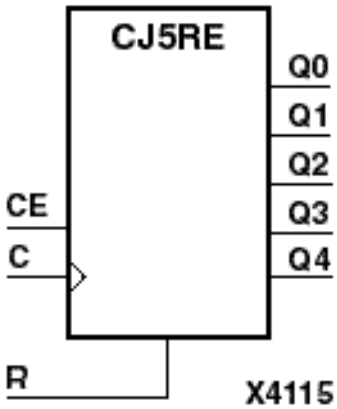


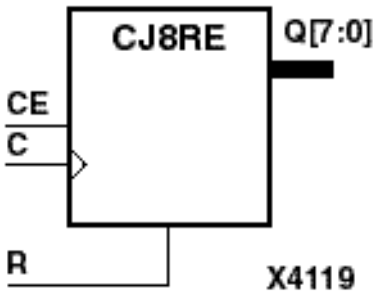
CJ4RE, CJ5RE, CJ8RE

4-, 5-, 8-Bit Johnson Counters with Clock Enable and Synchronous Reset

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro







CJ4RE, CJ5RE, and CJ8RE are resettable Johnson/shift counters. The synchronous reset (R) input, when High, overrides all other inputs and causes the data (Q) outputs to go to logic level zero during the Low-to-High clock (C) transition. The counter increments (shifts Q0 to Q1, Q1 to Q2, and so forth) when the clock enable input (CE) is High

during the Low-to-High clock transition. Clock transitions are ignored when CE is Low.

For CJ4RE, the Q3 output is inverted and fed back to input Q0 to provide continuous counting operation. For CJ5RE, the Q4 output is inverted and fed back to input Q0. For CJ8RE, the Q7 output is inverted and fed back to input Q0.

The counter is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs			**Outputs**			
R	**CE**	**C**	**Q0**	**Q1**	**Q2**	**Q3**
1	X	↑	0	0	0	0
0	0	X	No Chg	No Chg	No Chg	No Chg
0	1	↑	$\overline{q3}$	q0	q1	q2

q = state of referenced output one setup time prior to active clock transition

CJ4RE Truth Table

Inputs			**Outputs**				
R	**CE**	**C**	**Q0**	**Q1**	**Q2**	**Q3**	**Q4**
1	X	↑	0	0	0	0	0
0	0	X	No Chg	No Chg	No Chg	No Chg	No Chg
0	1	↑	$\overline{q4}$	q0	q1	q2	q3

q = state of referenced output one setup time prior to active clock transition

CJ5RE Truth Table

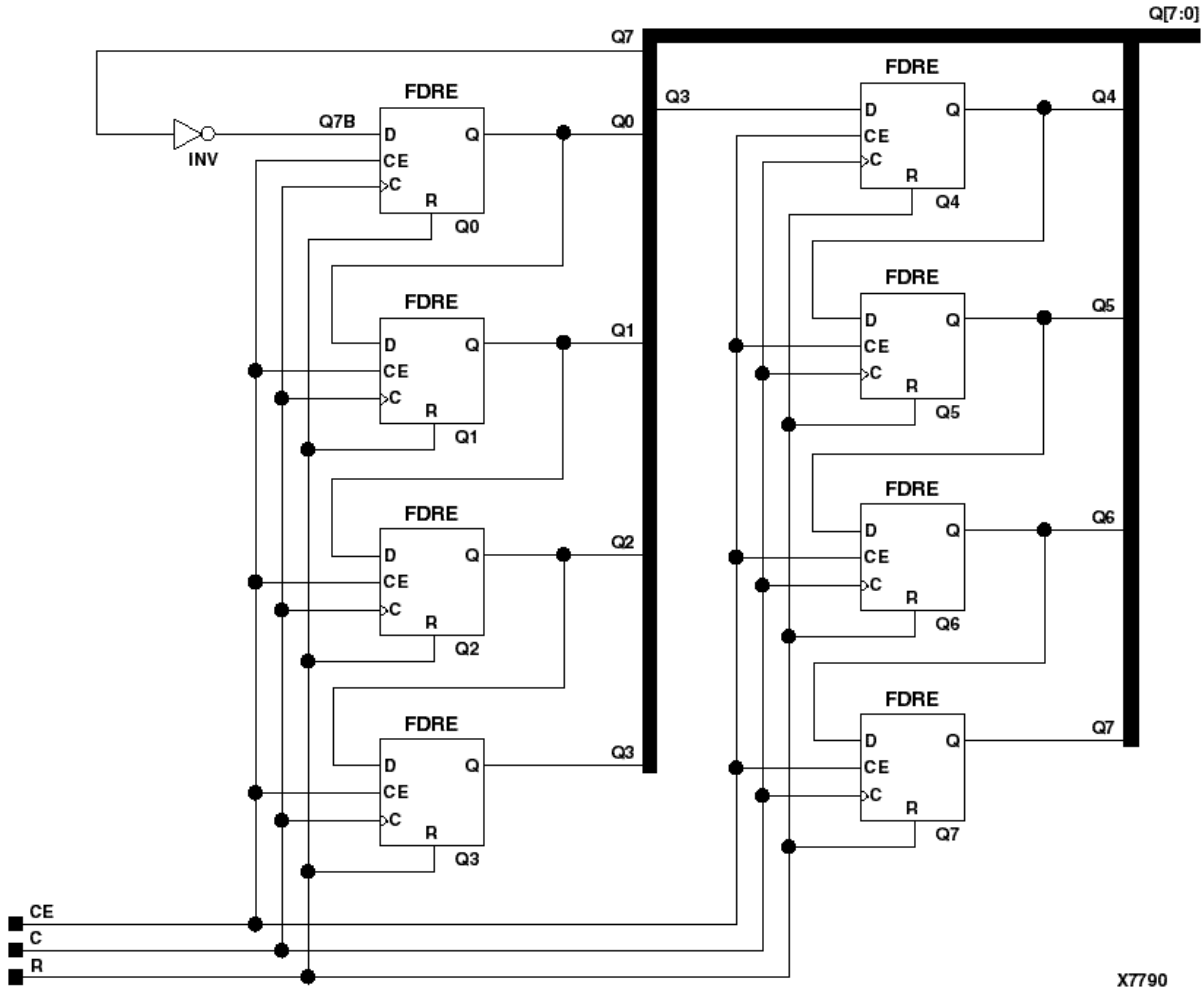
Inputs			**Outputs**

R	CE	C	Q0	Q1 – Q7
1	X	↑	0	0
0	0	X	No Chg	No Chg
0	1	↑	$\overline{q7}$	q0 – q6

q = state of referenced output one setup time prior to active clock transition

CJ8RE Truth Table

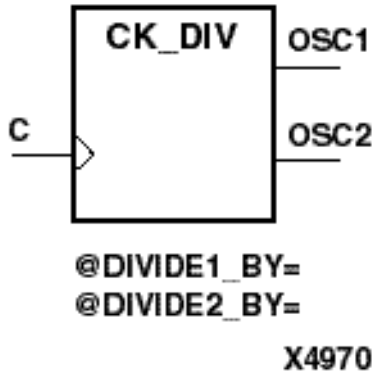
Figure 4-40CJ8RE Implementation XC3000, XC4000, XC5200, XC9000, Spartans, Virtex



CK_DIV

Internal Multiple-Frequency Clock Divider

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	N/A	Primitive	N/A	N/A	N/A	N/A



CK_DIV divides a user-provided external clock signal with different divide factors on either or both of the outputs. Only one CK_DIV may be used per design. The CK_DIV is not available if the OSC5 element is used.

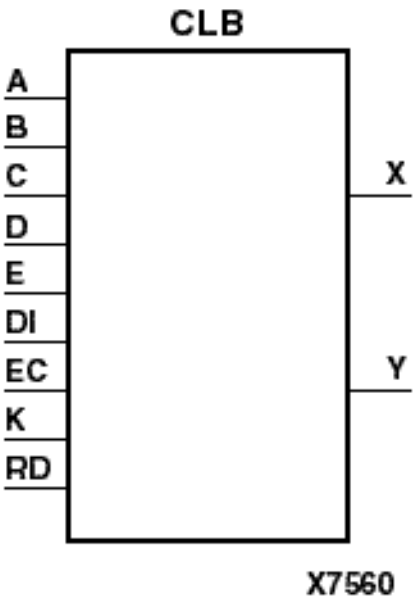
The clock frequencies of the OSC1 and OSC2 outputs are determined by specifying the DIVIDE1_BY=n_1 attribute for the OSC1 output and the DIVIDE2_BY=n_2 attribute for the OSC2 output. n_1 and n_2 are integer numbers by which the clock input (C) is divided to produce the desired output clock frequency. The available values of n_1 and n_2 are shown in the following table.

n_1	n_2
4	2
16	8
64	32
256	128
	1,024
	4,096
	16,384
	65,536

CLB

CLB Configuration Symbol

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Primitive	N/A	N/A	N/A	N/A	N/A	N/A	N/A



The CLB symbol enables you to manually specify a CLB configuration. It allows you to enter portions of a logic design directly in terms of the physical CLB, rather than schematically. Using the CLB symbol provides precise partitioning control and requires knowledge of the CLB architecture. Use it in place of the equivalent captured logic and not in conjunction with it.

A blank XC3000 CLB primitive symbol and its corresponding configured CLB primitive and circuit are shown in the following figure.

Figure 4-41XC3000 CLB Primitive Example and Equivalent Circuit

CLB

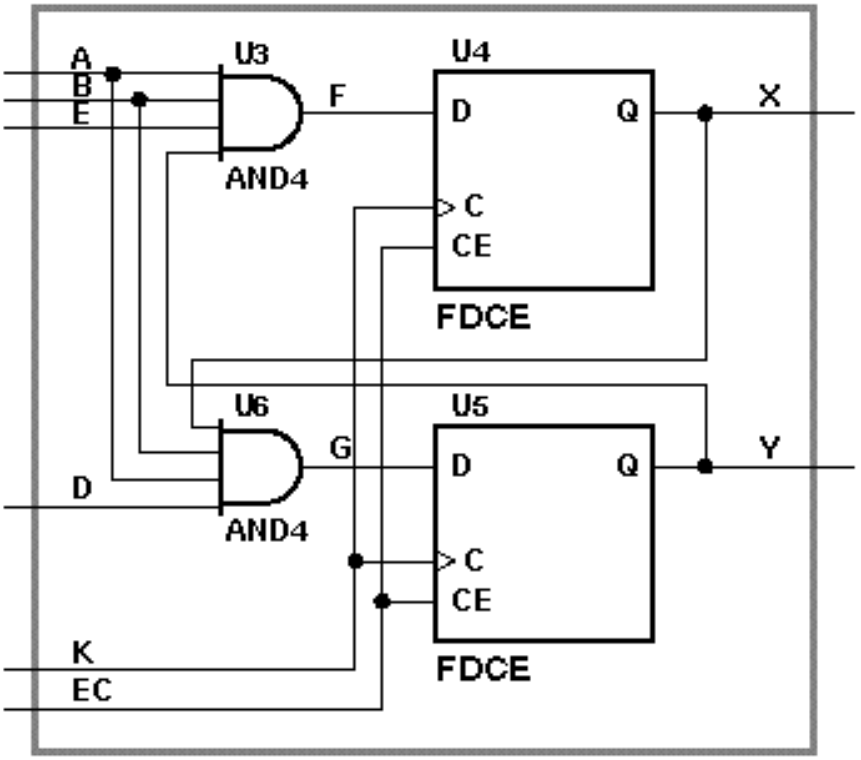
AA

FG

X:QX Y:QY DX:F DY:G CLK:K ENCLK:EC

F=A*B*E*QY

G=A*B*D*QX



X7234

CLB symbol pins correspond to actual CLB pins. Signals connected to these pins in a schematic are connected to the corresponding CLB pins in the design. You must specify the BASE, CONFIG, and EQUATE commands for the CLB. It is not necessary for the translator program to parse the commands specifying the CLB configuration. The mapping program from the LCA Xilinx netlist to the LCA design checks these commands for errors.

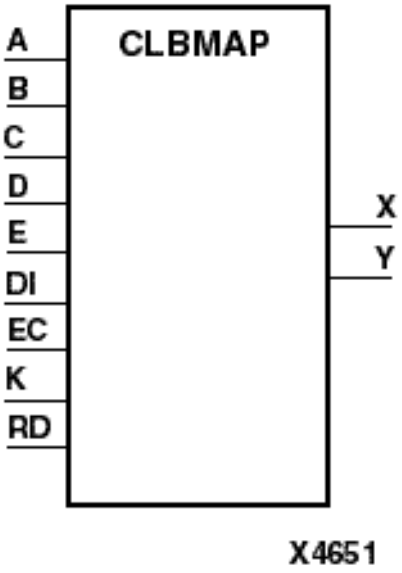
The configuration commands must be consistent with the connections. For example, if you use the A input in an equation, connect a signal to the A pin. Refer to the applicable CAE tool interface user guide for more information on specifying the CLB configuration commands in the schematic.

You can specify the location of a CLB on the device using the LOC attribute. When specifying the LOC attribute, a valid CLB name (AA, AB, and so forth) must be used. Refer to the **"LOC" section of the "Attributes, Constraints, and Carry Logic" chapter** for more information.

CLBMAP

Logic-Partitioning Control Symbol

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Primitive	N/A	N/A	N/A	N/A	N/A	N/A	N/A



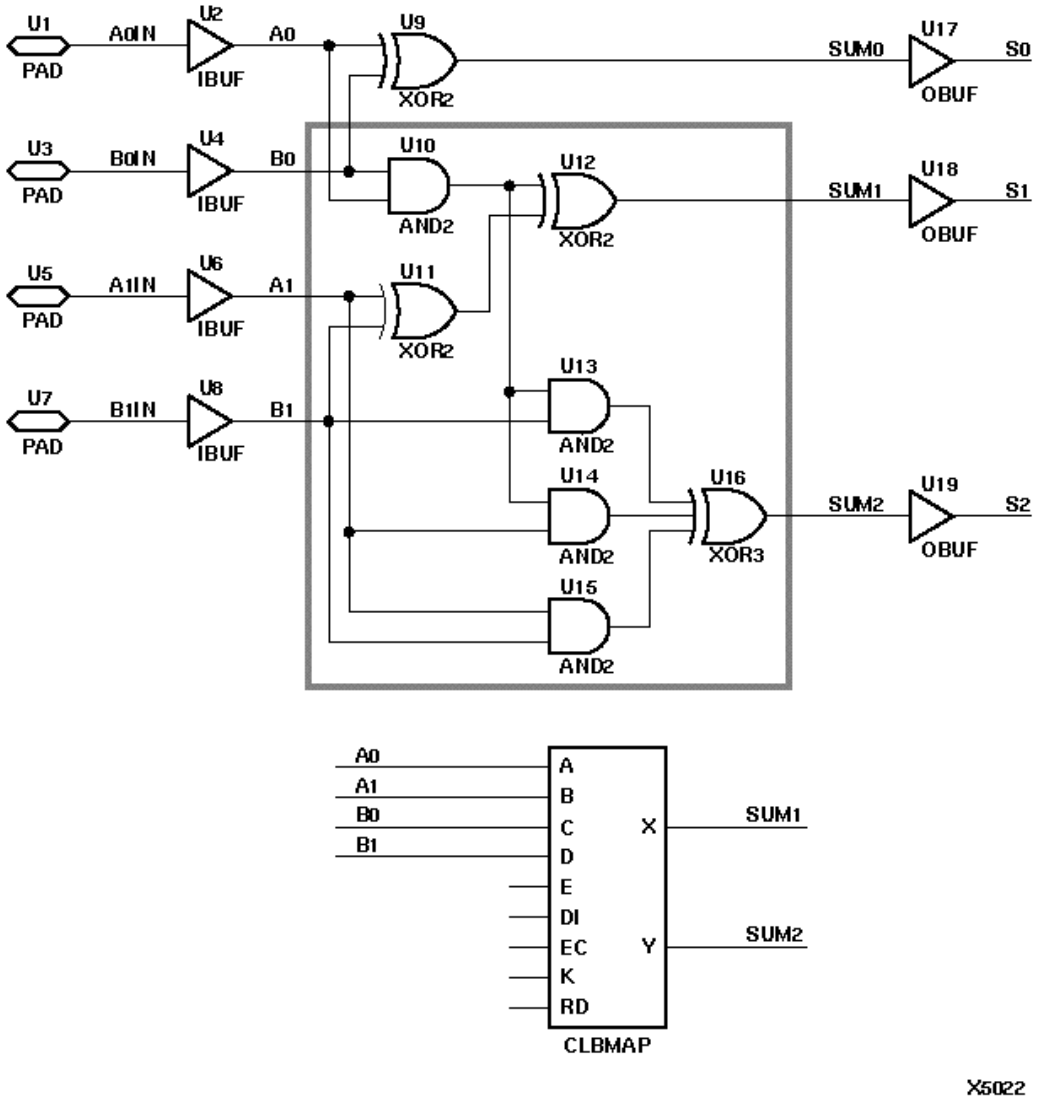
The CLBMAP symbol is used to control logic partitioning into XC3000 family CLBs. The CLBMAP symbol is not a substitute for logic. It is used in addition to combinational gates, latches, and flip-flops for mapping control.

At the schematic level, you can implement a portion of logic using gates, latches, and flip-flops and specify that the logic be grouped into a single CLB by using the CLBMAP symbol. You must name the signals that are the inputs and outputs of the CLB, then draw the signals to appropriate pins of the CLBMAP symbol, or name the CLBMAP signals and logic

signals correspondingly. The symbol can have unconnected pins, but all signals on the logic group to be mapped must be specified on a symbol pin.

CLBMAP primitives and equivalent circuits are shown for XC3000 families in the following figure.

Figure 4-42XC3000 CLBMAP Primitive Example and Equivalent



Use the MAP=*type* parameter with the CLBMAP symbol to further define how much latitude you want to give the mapping program. The following table shows MAP option characters and their meanings.

MAP Option	Function

Character	
P	Pins.
C	Closed — Adding logic to or removing logic from the CLB is not allowed.
L	Locked — Locking CLB pins.
O	Open — Adding logic to or removing logic from the CLB is allowed.
U	Unlocked — No locking on CLB pins.

Possible types of MAP parameters for FMAP are: MAP=PUC, MAP=PLC, MAP=PLO, and MAP=PUO. The default parameter is PUO. If one of the "open" parameters is used (PLO or PUO), only the output signals must be specified.

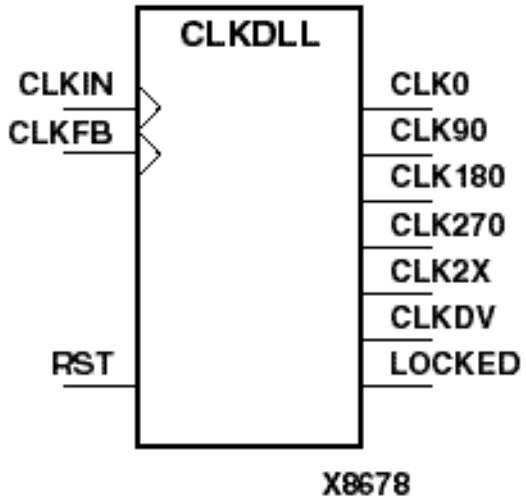
Note: Currently, only PUC and PUO are observed. PLC and PLO are translated into PUC and PUO, respectively.

You can lock individual pins using the "P" (Pin lock) parameter on the CLBMAP pin in conjunction with the PUC parameter. Refer to the appropriate CAE tool interface user guide for information on changing symbol parameters for your schematic editor.

CLKDLL

Clock Delay Locked Loop

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	N/A	N/A	N/A	N/A	N/A	Primitive



CLKDLL is a clock delay locked loop used to minimize clock skew. CLKDLL synchronizes the clock signal at the feed back clock input (CLKFB) to the clock signal at the input clock (CLKIN). The locked output (LOCKED) is high when the two signals are in phase. The signals are considered to be in phase when their rising edges are within 250 ps of each other.

The frequency of the clock signal at the CLKIN input must be in the range 30 - 120 MHz.

On-chip synchronization is achieved by connecting the CLKFB input to a point on the global clock network driven by a BUFG, a global clock buffer. The BUFG input can only be connected to the CLK0 or CLK2X output of CLKDLL. The BUFG connected to the CLKFB input of the CLKDLL must be sourced from either the CLK0 or CLK2X outputs of the same CLKDLL. The CLKIN input should be connected to the output of an IBUFG, with the IBUFG input connected to a pad driven by the system clock.

Off-chip synchronization is achieved by connecting the CLKFB input to the output of an IBUFG, with the IBUFG input connected to a pad. Only the CLK0 or CLK2X output can be used. The CLK0 or CLK2X must be connected to the input of OBUF, an output buffer.

The duty cycle of the CLK0 output is 50-50 unless the DUTY_CYCLE_CORRECTION attribute is set to FALSE, in which case the duty cycle is the same as that of the CLKIN input. The duty cycle of the phase shifted outputs (CLK90, CLK180, and CLK270) is the same as that of the CLK0 output. The duty cycle of the CLK2X and CLKDV outputs is always 50-50. The frequency of the CLKDV output is determined by the value assigned to the CLKDV_DIVIDE attribute.

The master reset input (RST) resets CLKDLL to its initial (power-on) state. The signal at the RST input is synchronized to the clock signal at the CLKIN input. The reset becomes effective at the second Low-to-High transition of the clock signal at the CLKIN input after assertion of the RST signal.

Table 4-1CLKDLL Outputs

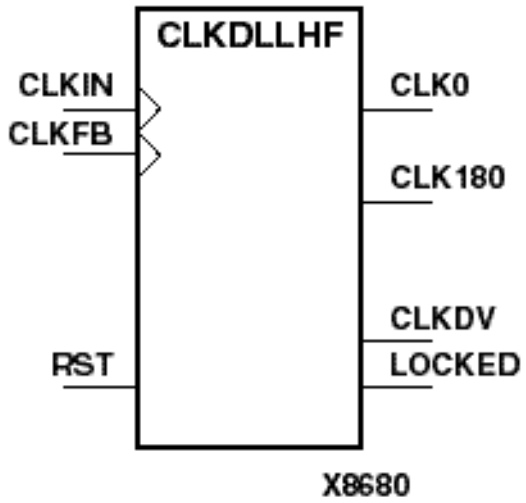
Output	Description
CLK0	Clock at 1x CLKIN frequency
CLK90	Clock at 1x CLKIN frequency, shifted 90^{o} with regards to CLK0

CLK180	Clock at 1x CLKIN frequency, shifted 180^{o} with regards to CLK0
CLK270	Clock at 1x CLKIN frequency, shifted 270^{o} with regards to CLK0
CLK2X	Clock at 2x CLKIN frequency
CLKDV	Clock at (1/n)x CLKIN frequency, n=CLKDV_DIVIDE value
LOCKED	CLKDLL locked

CLKDLLHF

High Frequency Clock Delay Locked Loop

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	N/A	N/A	N/A	N/A	N/A	Primitive



CLKDLLHF is a high frequency clock delay locked loop used to minimize clock skew. CLKDLLHF synchronizes the clock signal at the feed back clock input (CLKFB) to the clock signal at the input clock (CLKIN). The locked output (LOCKED) is high when the two signals are in phase. The signals are considered to be in phase when their rising edges are within 250 ps of each other.

The frequency of the clock signal at the CLKIN input must be in the range 60 - 180 MHz.

On-chip synchronization is achieved by connecting the CLKFB input to a point on the global clock network driven by a BUFG, a global clock buffer. The BUFG input can only be connected to the CLK0 output of CLKDLLHF. The BUFG connected to the CLKFB input of the CLKDLLHF must be sourced from the CLK0 output of the same CLKDLLHF.

The CLKIN input should be connected to the output of an IBUFG, with the IBUFG input connected to a pad driven by the system clock.

Off-chip synchronization is achieved by connecting the CLKFB input to the output of an IBUFG, with the IBUFG input connected to a pad. Only the CLK0 output can be used. CLK0 must be connected to the input of OBUF, an output buffer.

The duty cycle of the CLK0 output is 50-50 unless the DUTY_CYCLE_CORRECTION attribute is set to FALSE, in which case the duty cycle is the same as that of the CLKIN input. The duty cycle of the phase shifted output (CLK180) is the same as that of the CLK0 output. The frequency of the CLKDV output is determined by the value assigned to the CLKDV_DIVIDE attribute.

The master reset input (RST) resets CLKDLL to its initial (power-on) state. The signal at the RST input is synchronized to the clock signal at the CLKIN input. The reset becomes effective at the second Low-to-High transition of the clock signal at the CLKIN input after assertion of the RST signal.

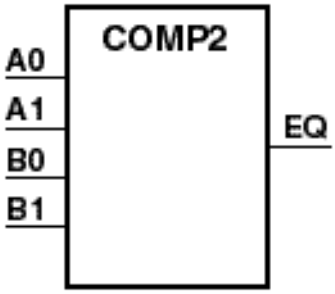
Table 4-2CLKDLLHF Outputs

Output	Description
CLK0	Clock at 1x CLKIN frequency
CLK180	Clock at 1x CLKIN frequency, shifted 180^{o} with regards to CLK0
CLKDV	Clock at (1/n)x CLKIN frequency, n=CLKDV_DIVIDE value
LOCKED	CLKDLL locked

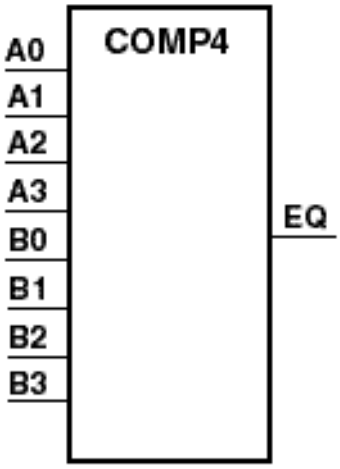
COMP2, 4, 8, 16

2-, 4-, 8-, 16-Bit Identity Comparators

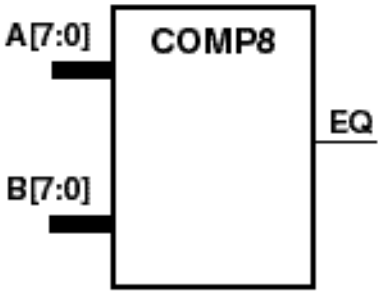
XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro



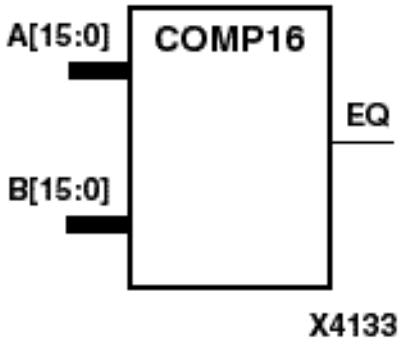
X4122



X4126



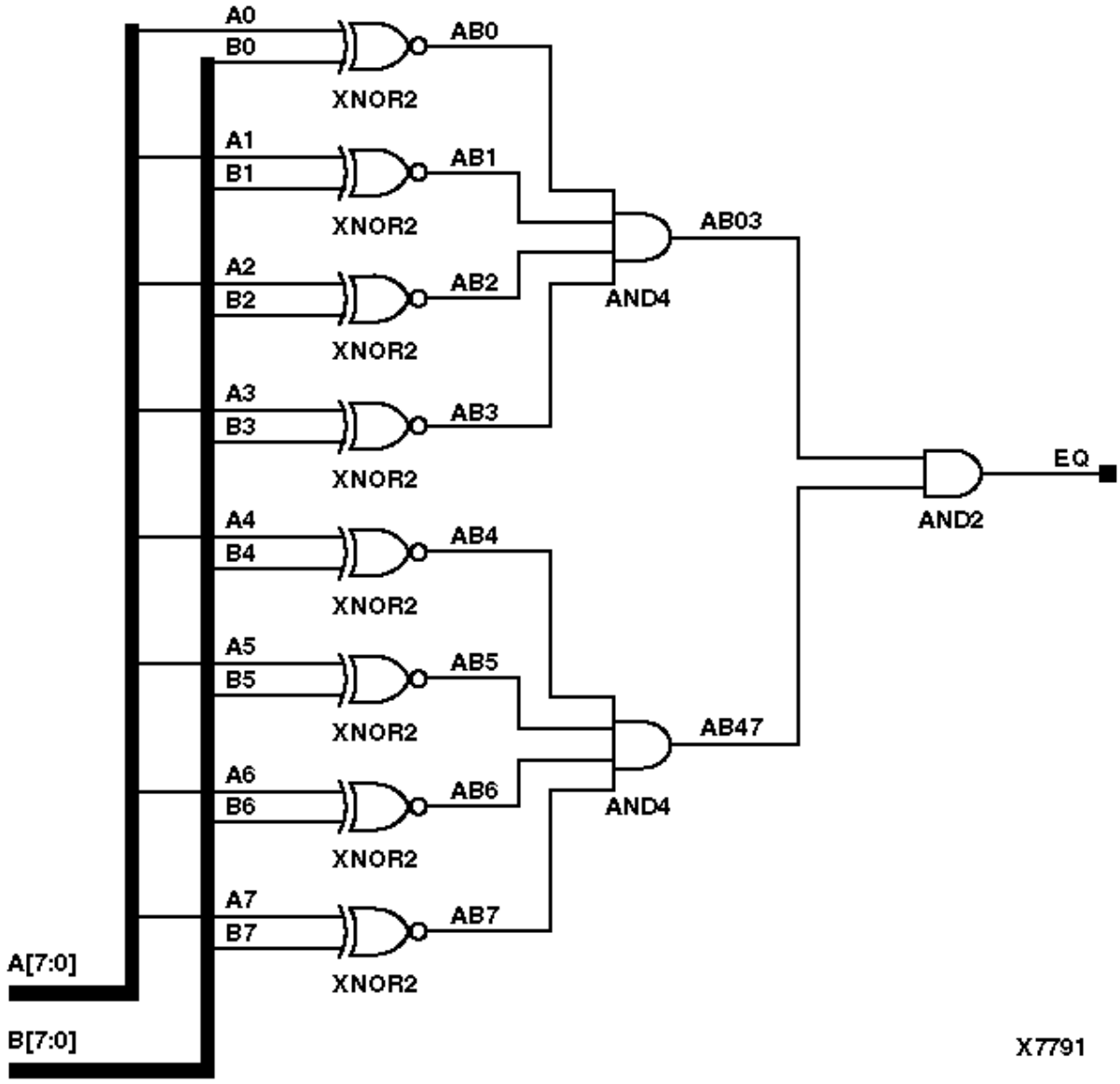
X4131



COMP2, COMP4, COMP8, and COMP16 are, respectively, 2-, 4-, 8-, and 16-bit identity comparators. The equal output (EQ) of the COMP2 2-bit, identity comparator is High when the two words A1 – A0 and B1 – B0 are equal. EQ is high for COMP4 when A3 – A0 and B3 – B0 are equal; for COMP8, when A7 – A0 and B7 – B0 are equal; and for COMP16, when A15 – A0 and B15 – B0 are equal.

Equality is determined by a bit comparison of the two words. When any two of the corresponding bits from each word are not the same, the EQ output is Low.

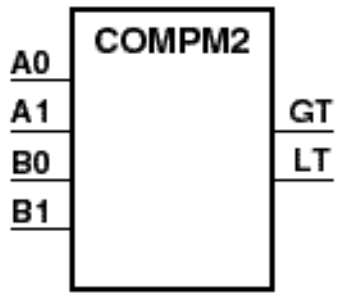
Figure 4-43COMP8 Implementation XC3000, XC4000, XC5200, XC9000, Spartans, Virtex



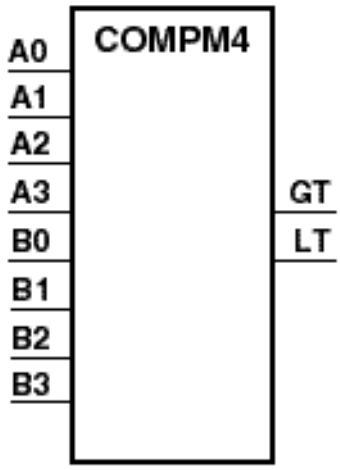
COMPM2, 4, 8, 16

2-, 4-, 8-, 16-Bit Magnitude Comparators

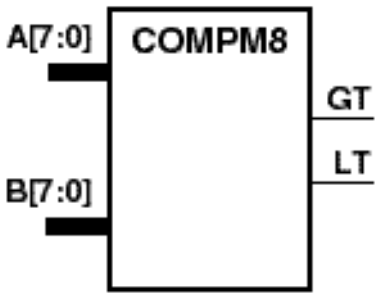
XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro



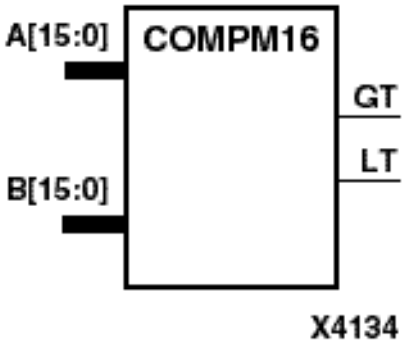
X4123



X4127



X4132



COMPM2, COMPM4, COMPM8, and COMPM16 are, respectively, 2-, 4-, 8-, and 16-bit magnitude comparators that compare two positive binary-weighted words.

COMPM2 compares A1 – A0 and B1 – B0, where A1 and B1 are the most significant bits. COMPM4 compares A3 – A0 and B3 – B0, where A3 and B3 are the most significant bits. COMPM8 compares A7 – A0 and B7 – B0, where A7 and B7 are the most significant bits. COMPM16 compares A15 – A0 and B15 – B0, where A15 and B15 are the most significant bits.

The greater-than output (GT) is High when A>B, and the less-than output (LT) is High when A<B. When the two words are equal, both GT and LT are Low. Equality can be measured with this macro by comparing both outputs with a NOR gate.

Inputs				Outputs	
A1	**B1**	**A0**	**B0**	**GT**	**LT**
0	0	0	0	0	0
0	0	1	0	1	0
0	0	0	1	0	1
0	0	1	1	0	0
1	1	0	0	0	0
1	1	1	0	1	0
1	1	0	1	0	1
1	1	1	1	0	0
1	0	X	X	1	0
0	1	X	X	0	1

COMPM2 Truth Table

Inputs				Outputs	
A3, B3	**A2, B2**	**A1, B1**	**A0, B0**	**GT**	**LT**
A3>B3	X	X	X	1	0
A3<B3	X	X	X	0	1
A3=B3	A2>B2	X	X	1	0
A3=B3	A2<B2	X	X	0	1
A3=B3	A2=B2	A1>B1	X	1	0
A3=B3	A2=B2	A1<B1	X	0	1
A3=B3	A2=A2	A1=B1	A0>B0	1	0
A3=B3	A2=B2	A1=B1	A0<B0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	0	0

COMPM4 Truth Table

Inputs								Outputs	
A7, B7	**A6, B6**	**A5, B5**	**A4, B4**	**A3, B3**	**A2, B2**	**A1, B1**	**A0, B0**	**GT**	**LT**
A7> B7	X	X	X	X	X	X	X	1	0
A7< B7	X	X	X	X	X	X	X	0	1
A7= B7	A6> B6	X	X	X	X	X	X	1	0
A7= B7	A6< B6	X	X	X	X	X	X	0	1
A7= B7	A6= B6	A5> B5	X	X	X	X	X	1	0
A7= B7	A6= B6	A5< B5	X	X	X	X	X	0	1
A7= B7	A6= B6	A5= B5	A4> B4	X	X	X	X	1	0
A7= B7	A6= B6	A5= B5	A4< B4	X	X	X	X	0	1

A7= B7	A6= B6	A5= B5	A4= B4	A3> B3	X	X	X	1	0
A7= B7	A6= B6	A5= B5	A4= B4	A3< B3	X	X	X	0	1
A7= B7	A6= B6	A5= B5	A4= B4	A3= B3	A2> B2	X	X	1	0
A7= B7	A6= B6	A5= B5	A4= B4	A3= B3	A2< B2	X	X	0	1
A7= B7	A6= B6	A5= B5	A4= B4	A3= B3	A2= B2	A1> B1	X	1	0
A7= B7	A6= B6	A5= B5	A4= B4	A3= B3	A2= B2	A1< B1	X	0	1
A7= B7	A6= B6	A5= B5	A4= B4	A3= B3	A2= B2	A1= B1	A0> B0	1	0
A7= B7	A6= B6	A5= B5	A4= B4	A3= B3	A2= B2	A1= B1	A0< B0	0	1
A7= B7	A6= B6	A5= B5	A4= B4	A3= B3	A2= B2	A1= B1	A0= B0	0	0

COMPM8 Truth Table (also representative of COMPM16)

Figure 4-44COMPM8 Implementation XC3000, XC4000, XC5200, Spartans, Virtex

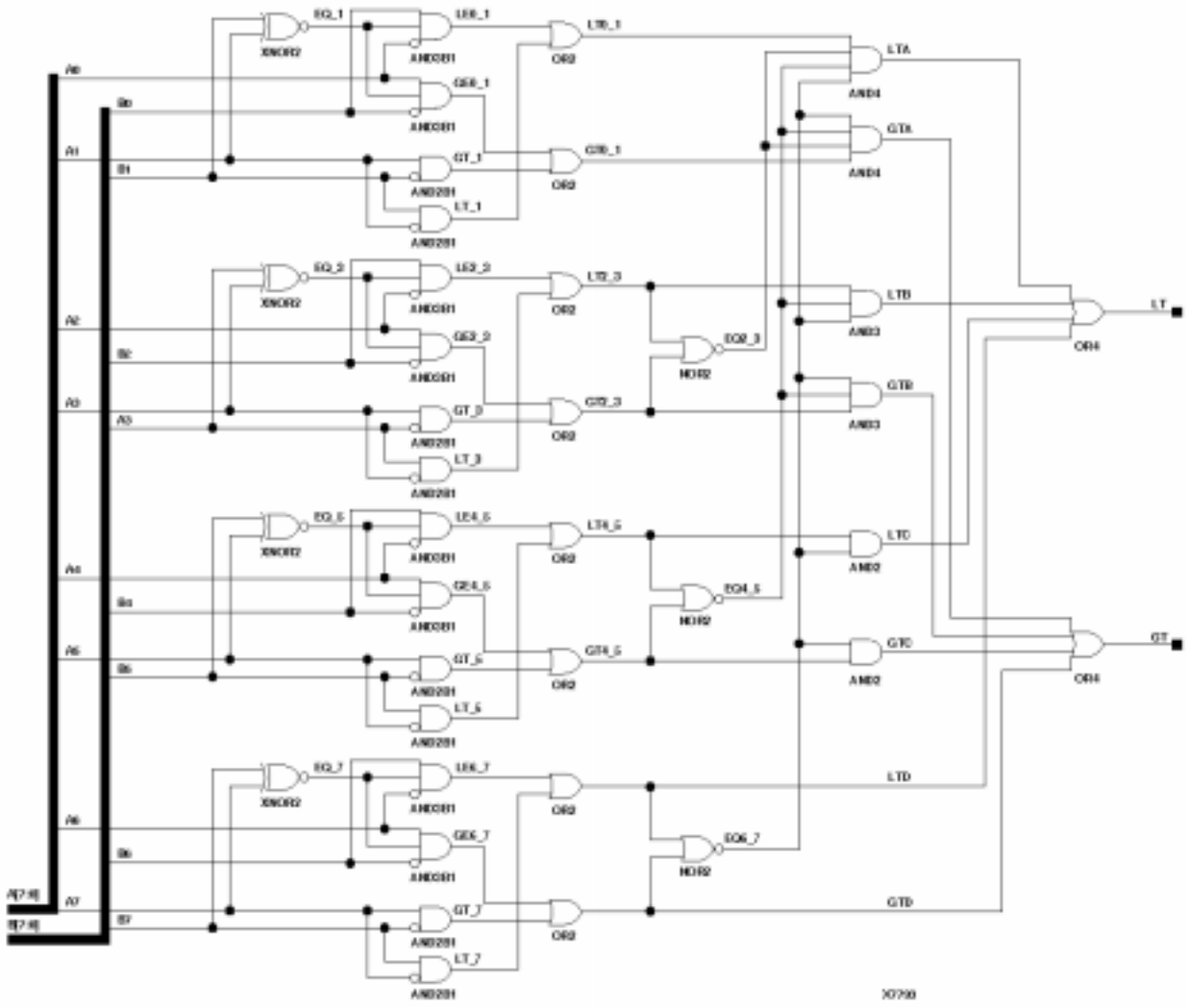
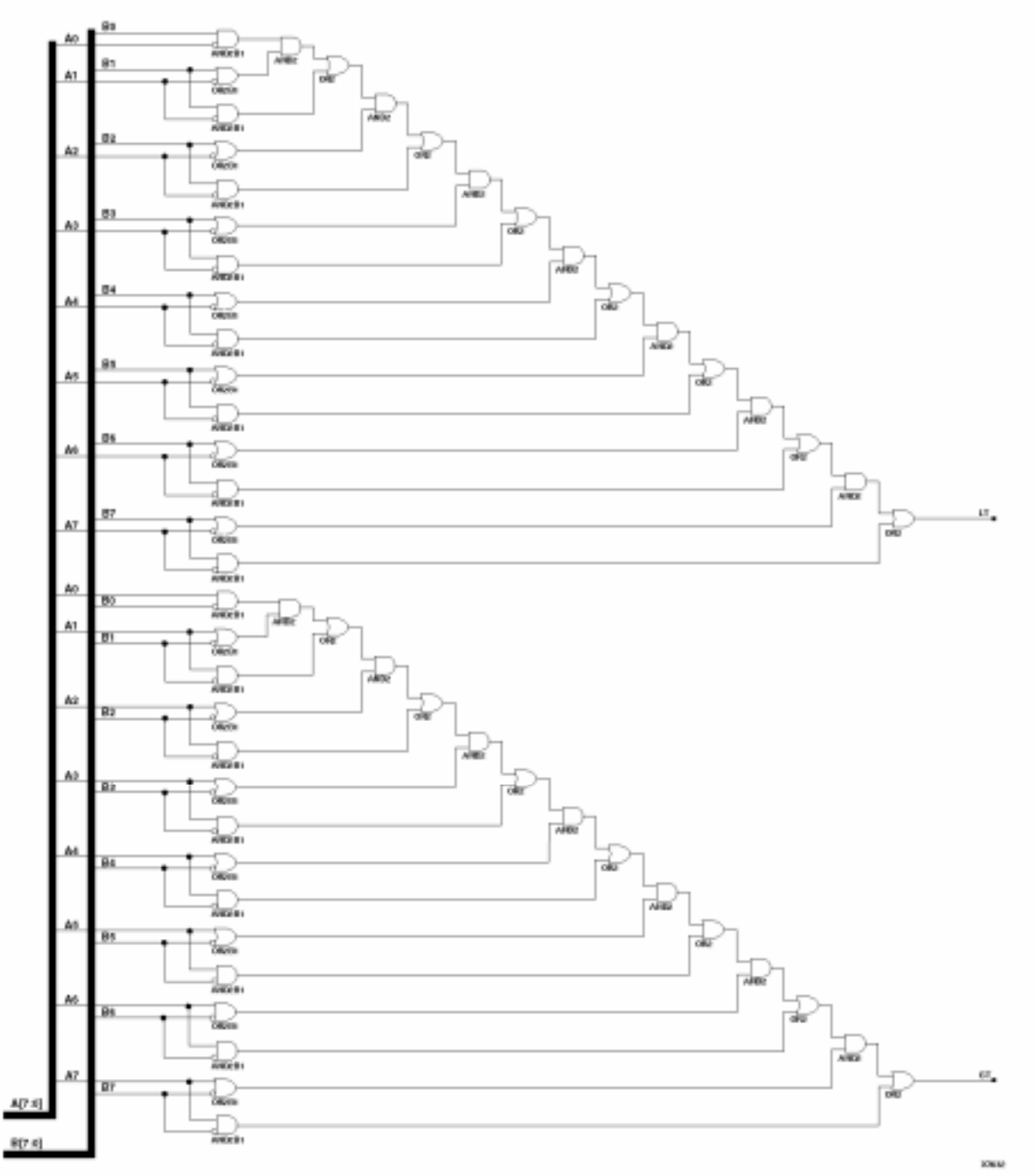


Figure 4-45COMPM8 Implementation XC9000

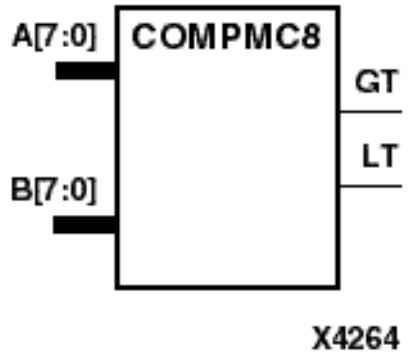


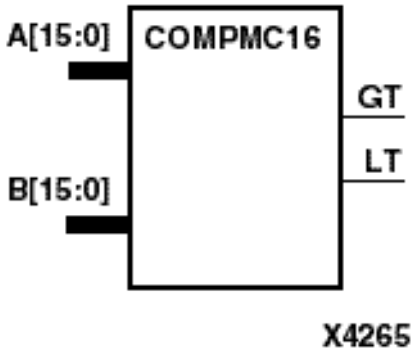
COMPMC8, 16

8-, 16-Bit Magnitude Comparators

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex

N/A	Macro	Macro	Macro	N/A	Macro	Macro	Macro





COMPMC8 is an 8-bit, magnitude comparator that compares two positive binary-weighted words A7 – A0 and B7 – B0, where A7 and B7 are the most significant bits. COMPMC16 is a 16-bit, magnitude comparator that compares two positive binary-weighted words A15 – A0 and B15 – B0, where A15 and B15 are the most significant bits.

These comparators are implemented using carry logic with relative location constraints to ensure efficient logic placement.

The greater-than output (GT) is High when A>B, and the less-than output (LT) is High when A<B. When the two words are equal, both GT and LT are Low. Equality can be flagged with this macro by connecting both outputs to a NOR gate.

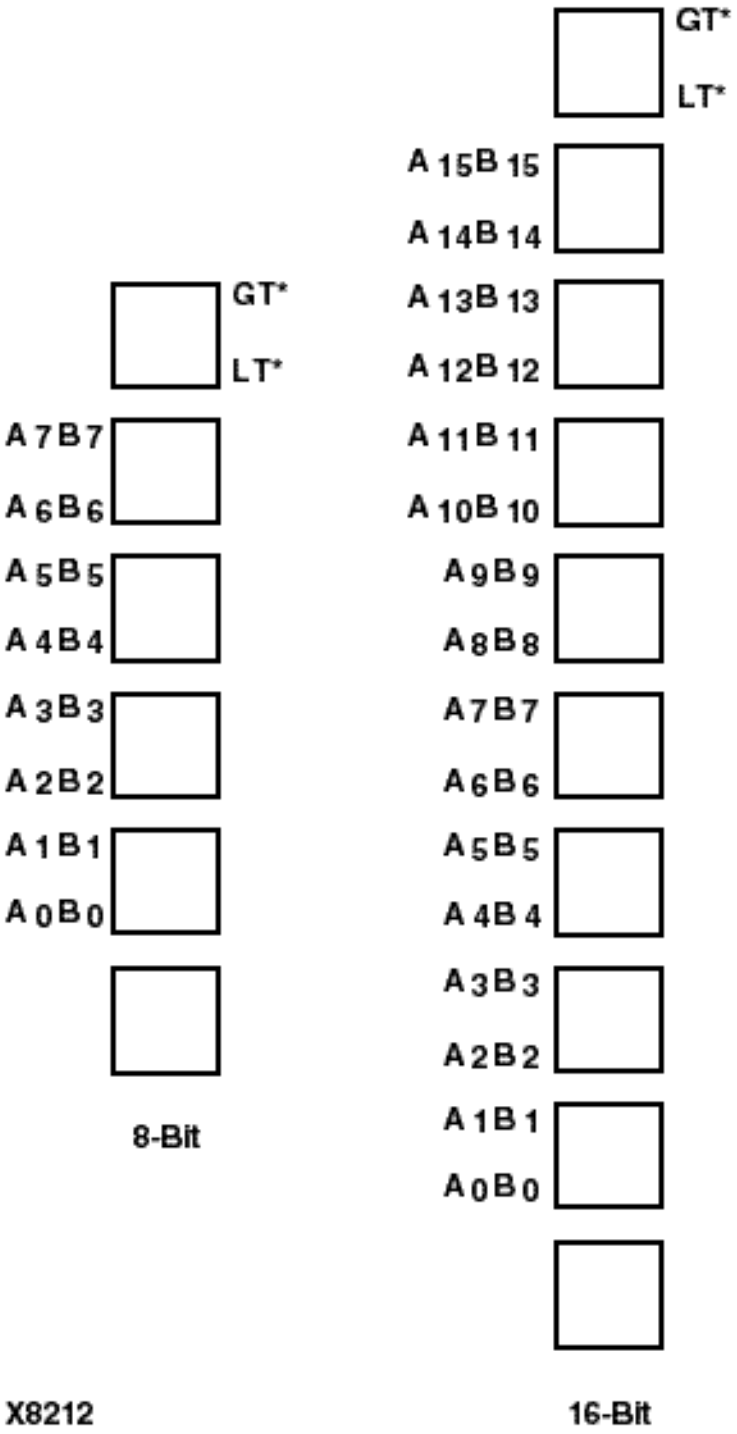
Inputs								**Outputs**	
A7, B7	**A6, B6**	**A5, B5**	**A4, B4**	**A3, B3**	**A2, B2**	**A1, B1**	**A0, B0**	**GT**	**LT**
A7> B7	X	X	X	X	X	X	X	1	0
A7<	X	X	X	X	X	X	X	0	1

B7									
A7=B7	A6>B6	X	X	X	X	X	X	1	0
A7=B7	A6<B6	X	X	X	X	X	X	0	1
A7=B7	A6=B6	A5>B5	X	X	X	X	X	1	0
A7=B7	A6=B6	A5<B5	X	X	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4>B4	X	X	X	X	1	0
A7=B7	A6=B6	A5=B5	A4<B4	X	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3>B3	X	X	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3<B3	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2>B2	X	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2<B2	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1>B1	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1<B1	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0>B0	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0<B0	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0=B0	0	0

COMPMC8 Truth Table (also representative of COMPMC16)

Topology for XC4000 and Spartans

This is the COMPMC8 (8-bit) and COMPMC16 (16-bit) topology for XC4000 and Spartan series devices.



In the process of combining the logic that loads GT and LT, the place and route software might map the logic that generates GT and LT to different function generators. If this mapping occurs, the GT and LT logic cannot be placed in the uppermost CLB, as indicated in the illustration.

Figure 4-46COMPMC8 Implementation XC4000, Spartans

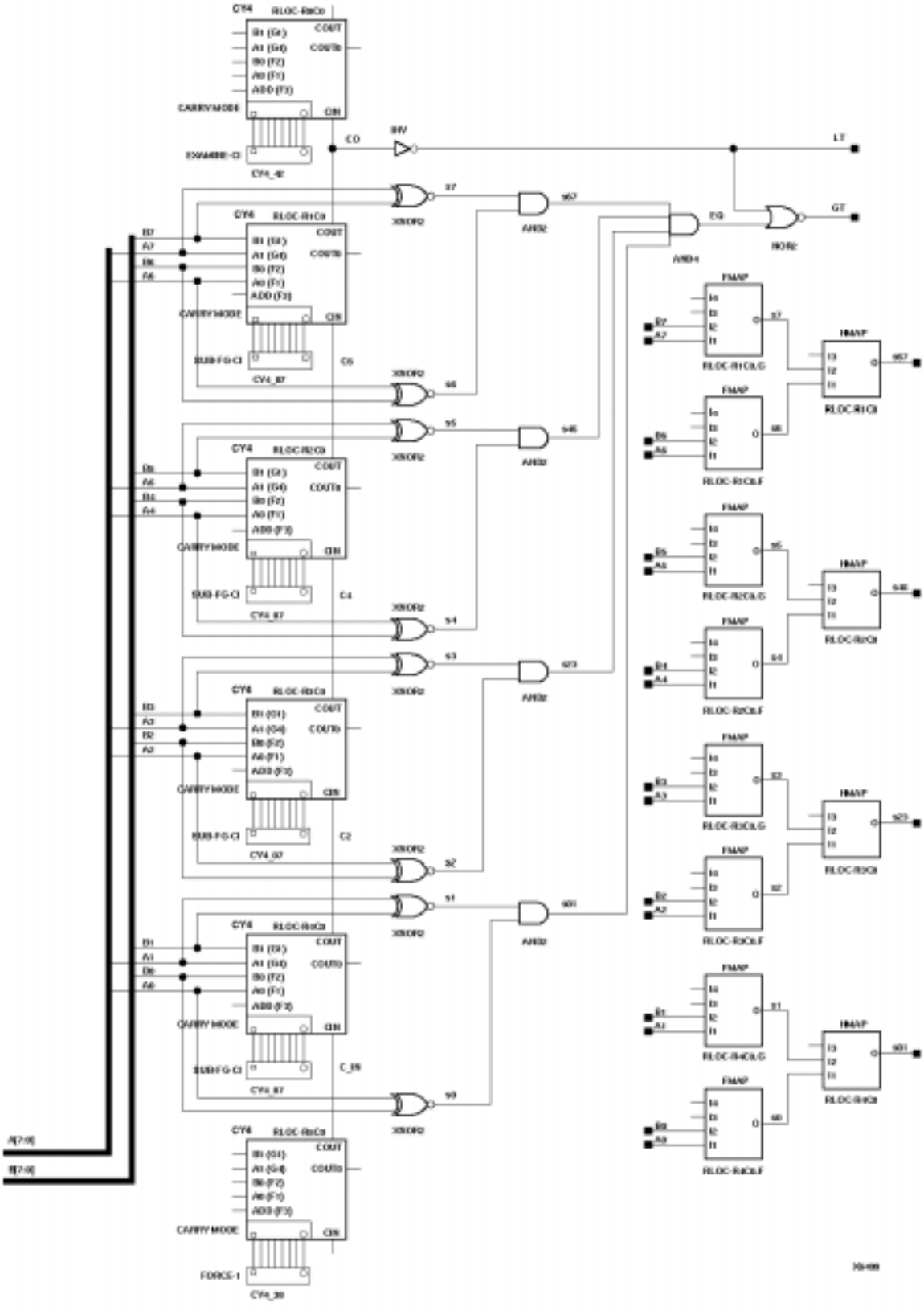


Figure 4-47COMPMC8 Implementation XC5200

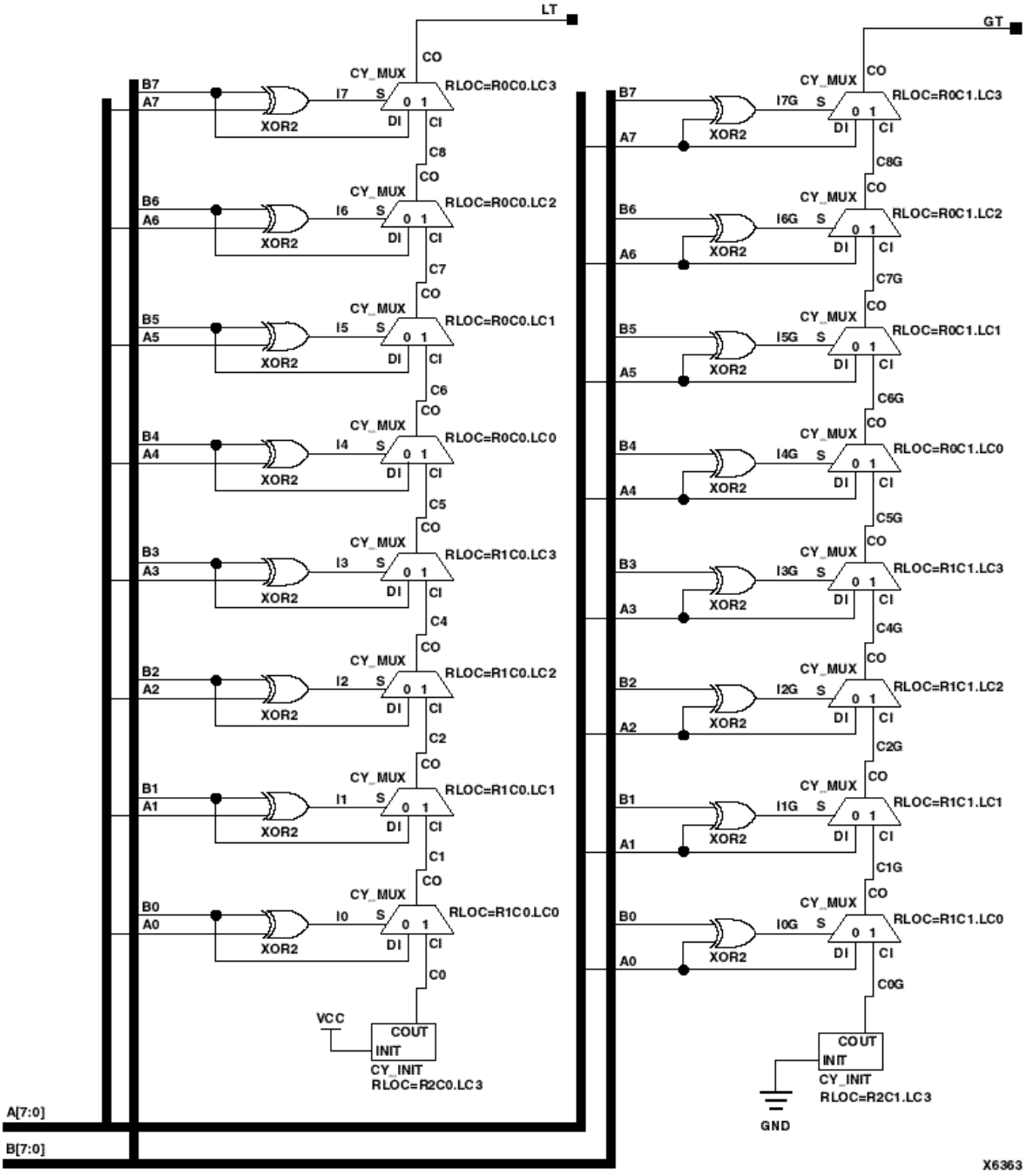
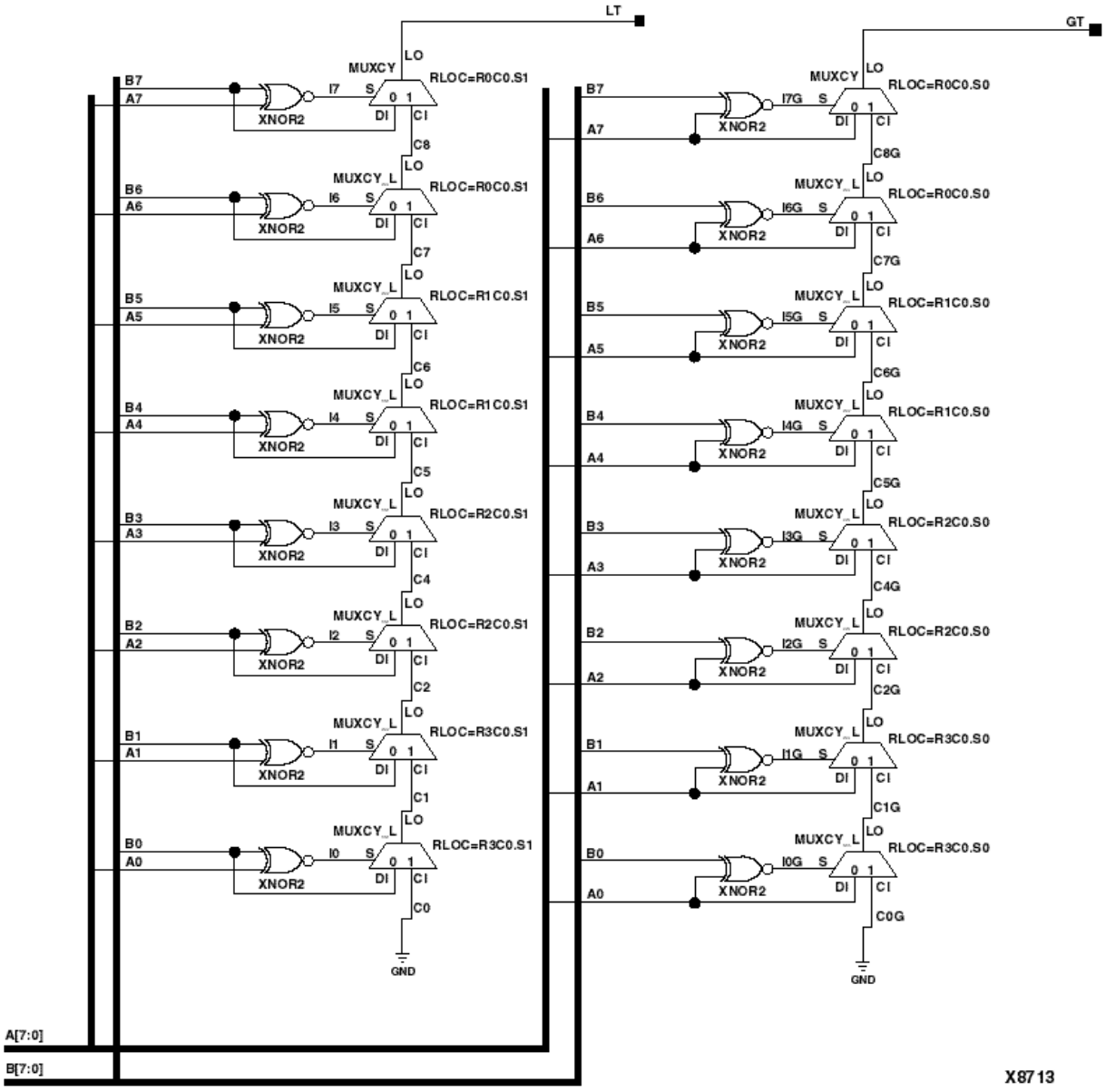


Figure 4-48COMPMC8 Implementation Virtex



CONFIG

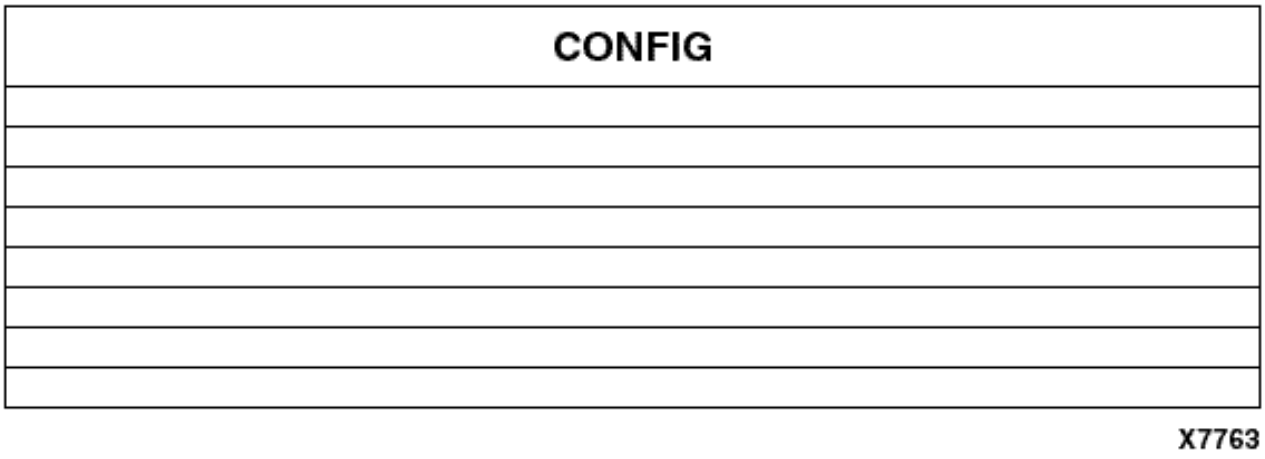
Repository for Schematic-Level (Global) Attributes

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive

The CONFIG primitive is a table that you can use to specify up to eight attributes that affect the entire design (global

attributes such as **PART** or **PROHIBIT**).

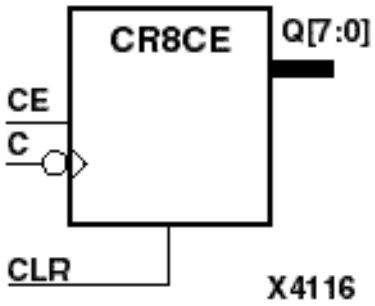
When using certain CAE software packages, global properties cannot be attached to the "Schematic" or "Sheet." Instead, they must be attached to the CONFIG symbol. Enter attributes using the same syntax that you would use in a UCF file. The global attributes can be any length, but only 30 characters are displayed in the CONFIG window. The CONFIG table is shown in the following figure.

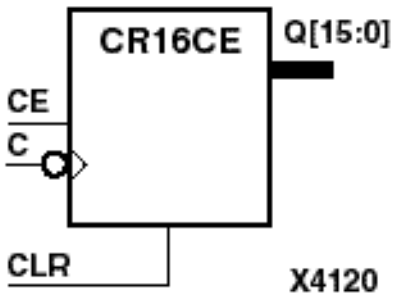


CR8CE, CR16CE

8-, 16-Bit Negative-Edge Binary Ripple Counters with Clock Enable and Asynchronous Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro





CR8CE and CR16CE are 8-bit and 16-bit, cascadable, clearable, binary, ripple counters. The asynchronous clear (CLR), when High, overrides all other inputs and causes the Q outputs to go to logic level zero. The counter increments when the clock enable input (CE) is High during the High-to-Low clock (C) transition. The counter ignores clock transitions when CE is Low.

Larger counters can be created by connecting the last Q output (Q7 for CR8CE, Q15 for CR16CE) of the first stage to the clock input of the next stage. CLR and CE inputs are connected in parallel. The clock period is not affected by the overall length of a ripple counter. The overall clock-to-output propagation is $n(t_{C-Q})$, where n is the number of stages and the time t_{C-Q} is the C-to-Qz propagation delay of each stage.

The counter is asynchronously cleared, output Low, when power is applied. For CPLDs, the power-on condition can be simulated by applying a High-level pulse on the PRLD global net. FPGAs simulate power-on when global reset (GR) or global set/reset (GSR) is active. GR for XC3000 is active-Low. GR for XC5200 and GSR (XC4000, Spartans, Virtex) default to active-High but can be inverted by adding an inverter in front of the GR/GSR input of the STARTUP or STARTUP_VIRTEX symbol.

Inputs			**Outputs**
CLR	**CE**	**C**	**Qz – Q0**
1	X	X	0
0	0	X	No Chg
0	1	↓	Inc

z = 7 for CR8CE; z = 15 for CR16CE.

Figure 4-49CR8CE Implementation XC3000

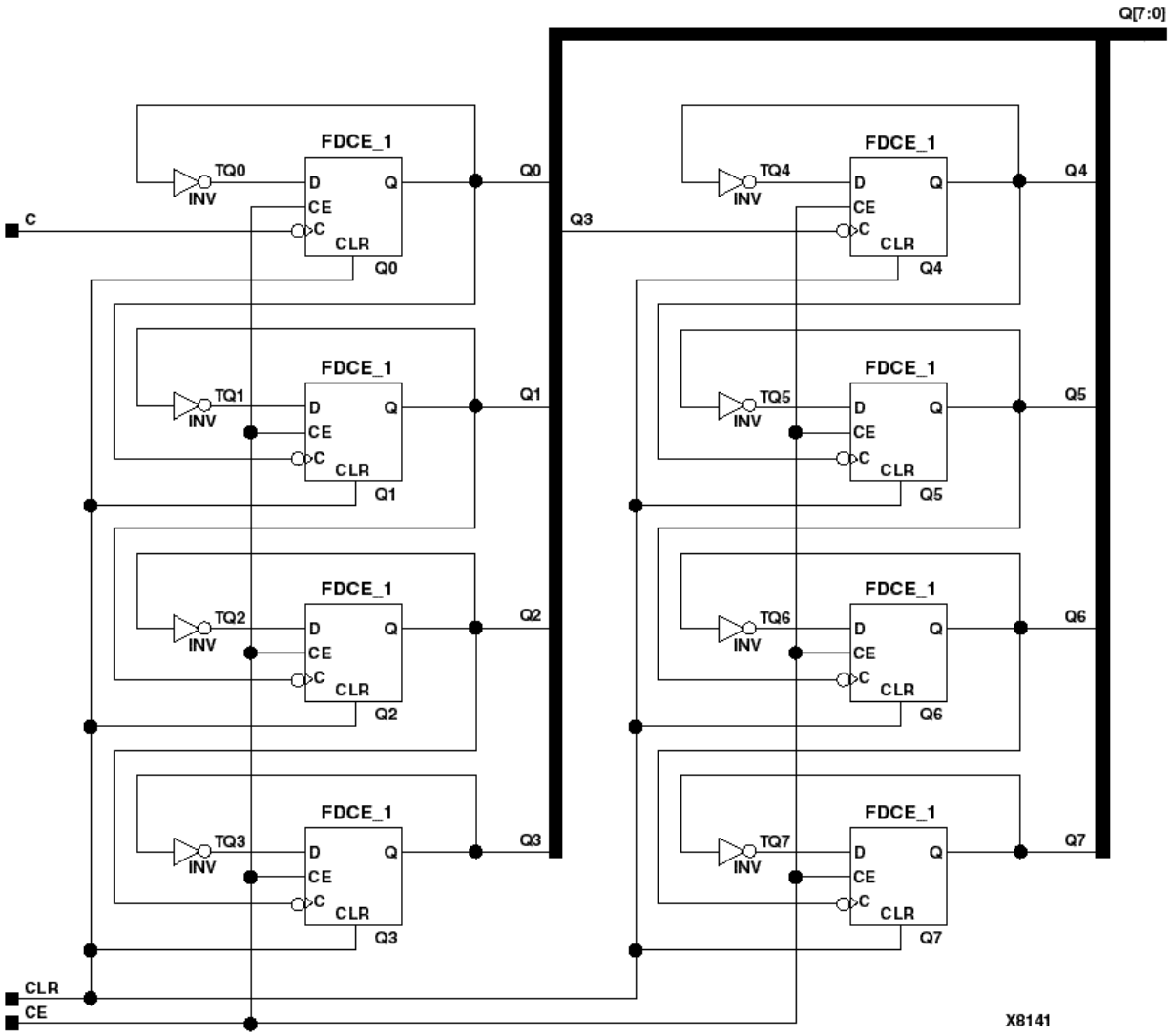


Figure 4-50CR8CE Implementation XC4000, XC5200, Spartans, Virtex

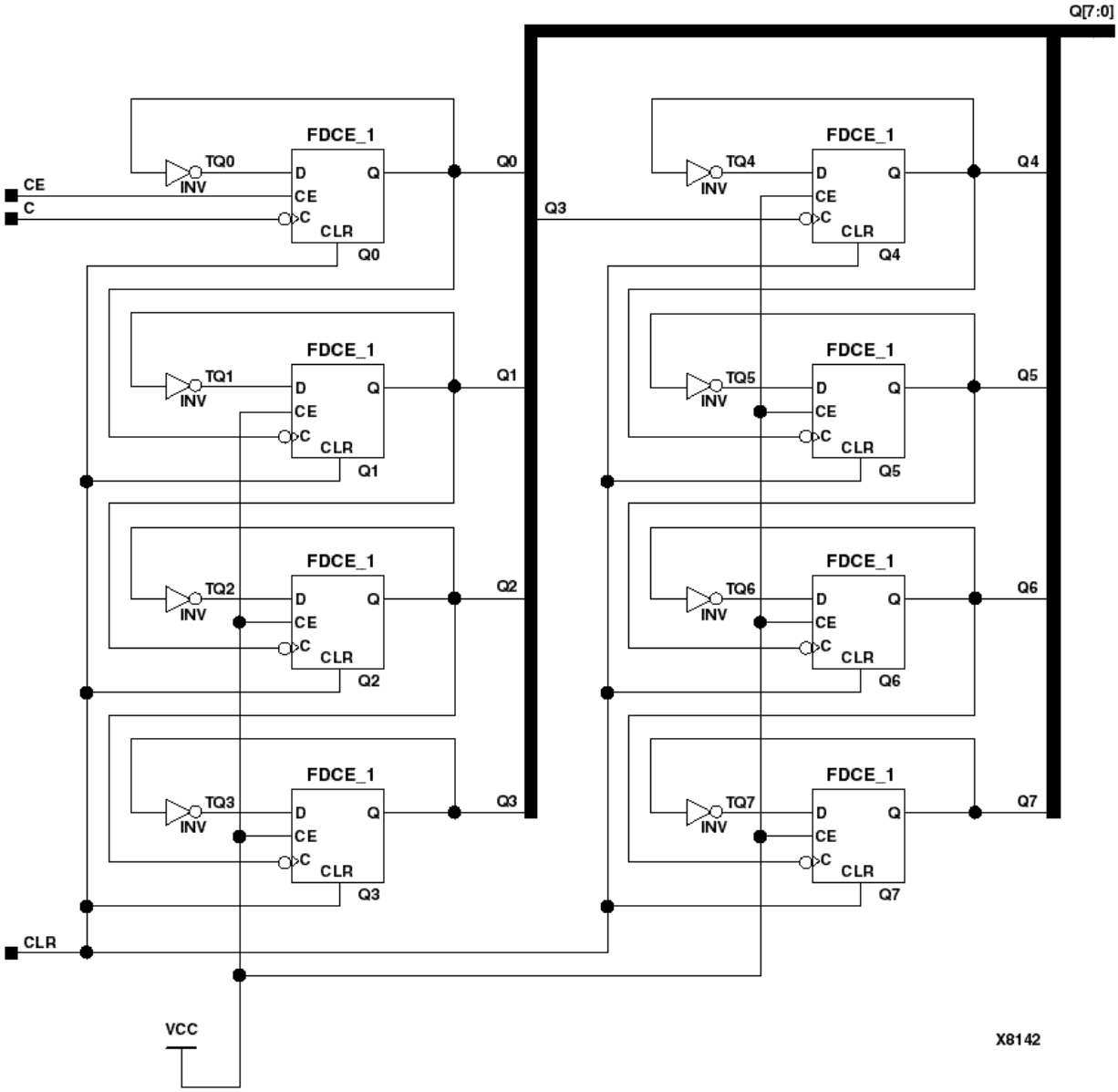
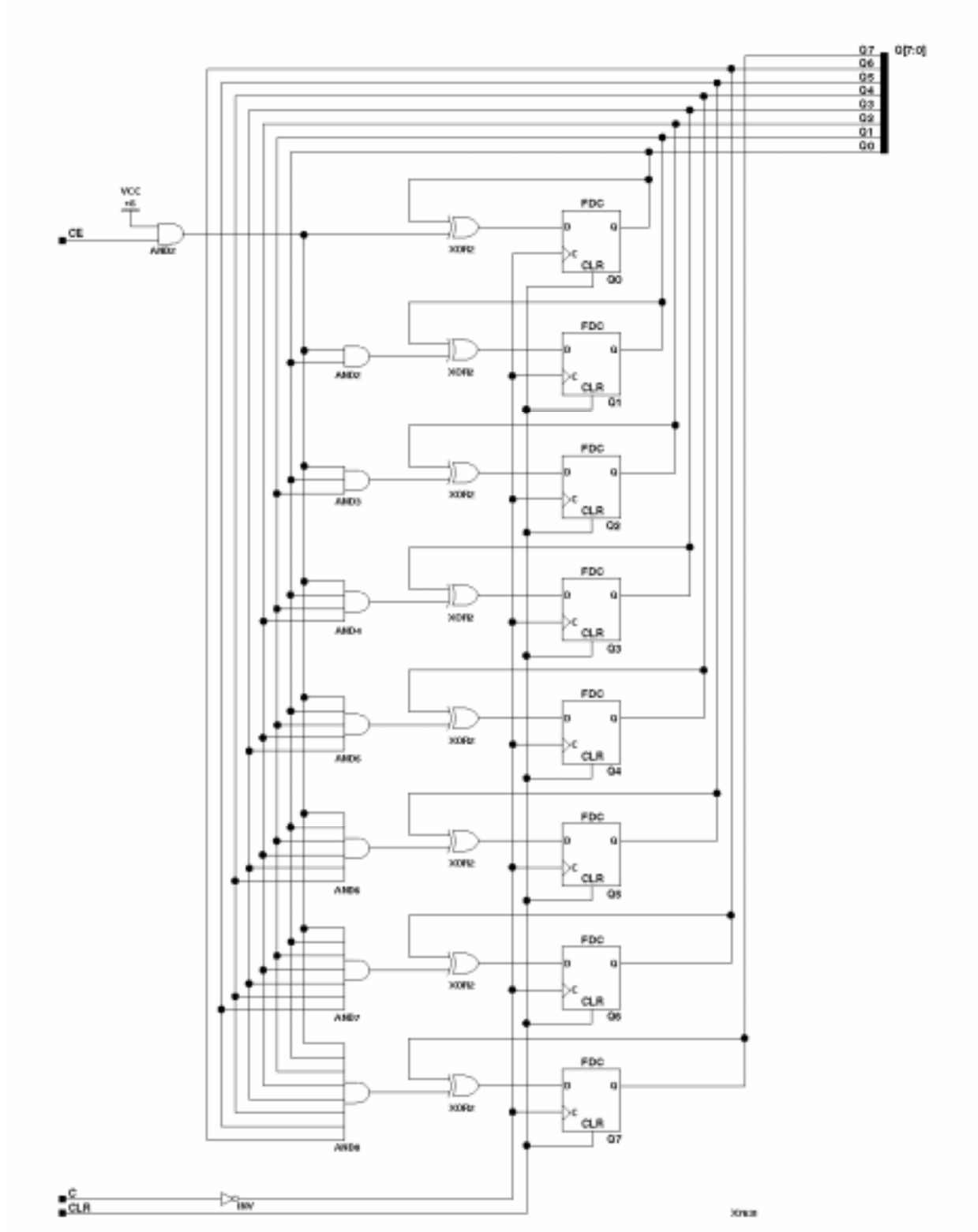


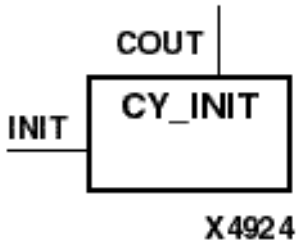
Figure 4-51CR8CE Implementation XC9000



CY_INIT

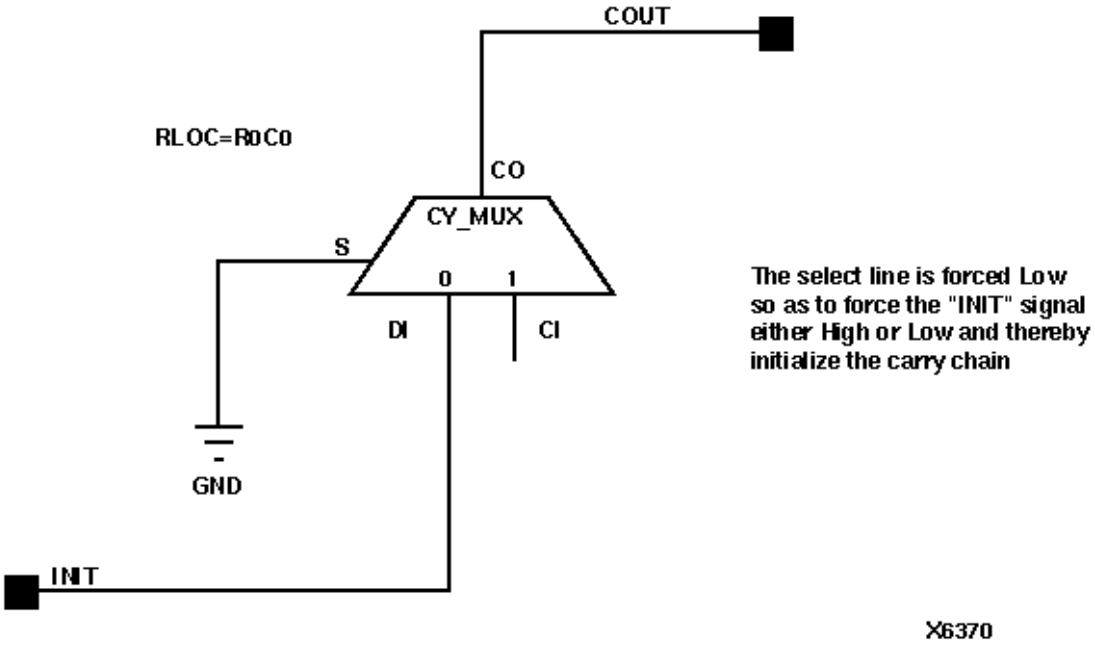
Initialization Stage for Carry Chain

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	N/A	Macro	N/A	N/A	N/A	N/A



CY_INIT is used to initialize the carry chain in the XC5200 architecture. It is used in conjunction with multiple CY_MUX elements to implement high speed carry-propagate or high speed cascade logic. CY_INIT must be placed in the logic cell (LC) immediately below the least-significant carry element (CY_MUX) in the carry/cascade chain. The INIT input is driven from the direct input (DI) to LC. The CY_INIT carry-out (COUT) drives the C_{in} input of the first LC in the carry chain. The COUT output reflects the state of the DI input. This figure represents the schematic implementation of CY_INIT.

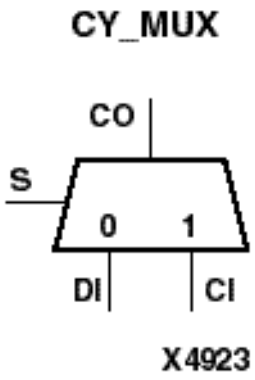
Figure 4-52CY _INIT 4-Bit Adder Implementation XC5200



CY_MUX

2-to-1 Multiplexer for Carry Logic

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	N/A	Primitive	N/A	N/A	N/A	N/A

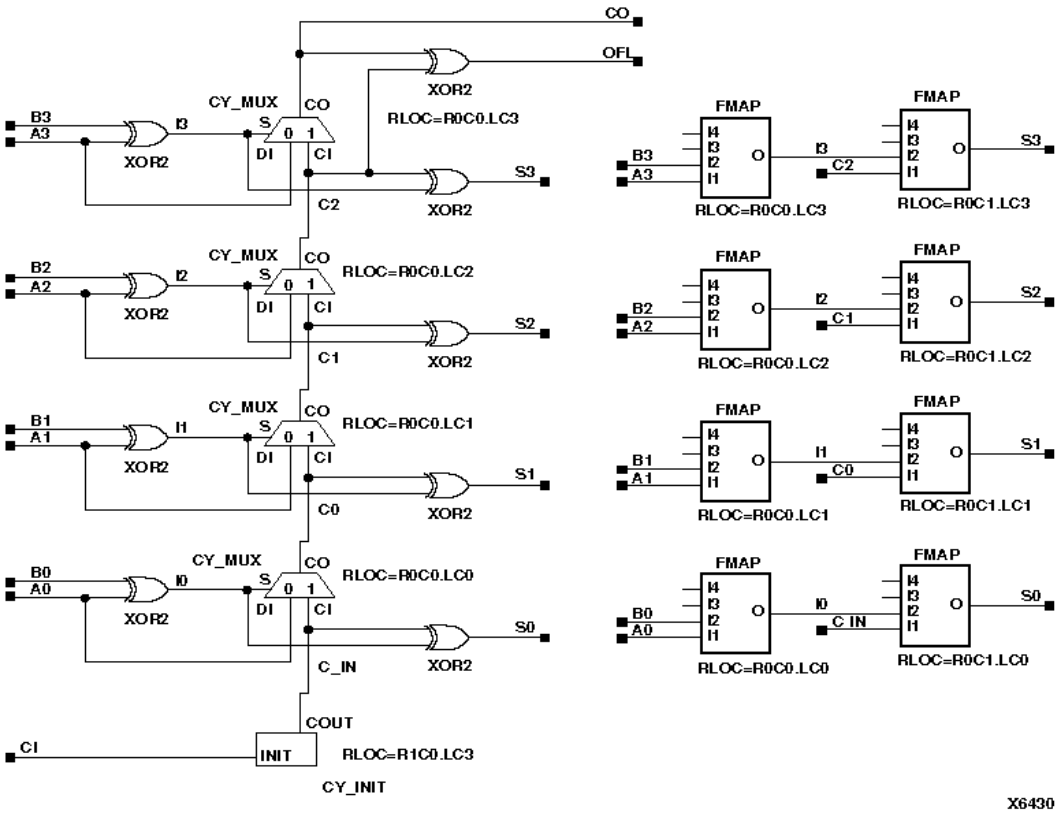


CY_MUX is used to implement a 1-bit high-speed carry propagate function. One such function can be implemented per logic cell (LC), for a total of 4-bits per configurable logic block (CLB). The direct input (DI) of an LC is connected to the DI input of the CY_MUX. The carry in (CI) input of an LC is connected to the CI input of the CY_MUX. The select input (S) of the CY_MUX is driven by the output of the lookup table (LUT) and configured as an XOR function. The carry out (CO) of the CY_MUX reflects the state of the selected input and implements the carry out function of each LC. When Low, S selects DI; when High, S selects CI.

Inputs			Outputs
S	**DI**	**CI**	**CO**
0	1	X	1
0	0	X	0
1	X	1	1
1	X	0	0

The following figure depicts the application of the CY_MUX for a 4-bit adder. Also shown are the associated FMAP symbols and the CY_INIT function.

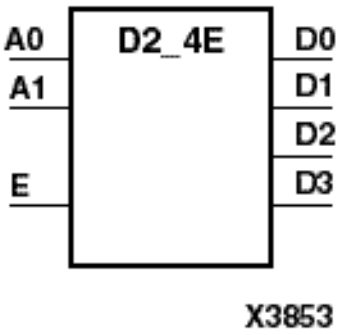
Figure 4-53CY_MUX 4-Bit Adder Schematic XC5200



D2_4E

2- to 4-Line Decoder/Demultiplexer with Enable

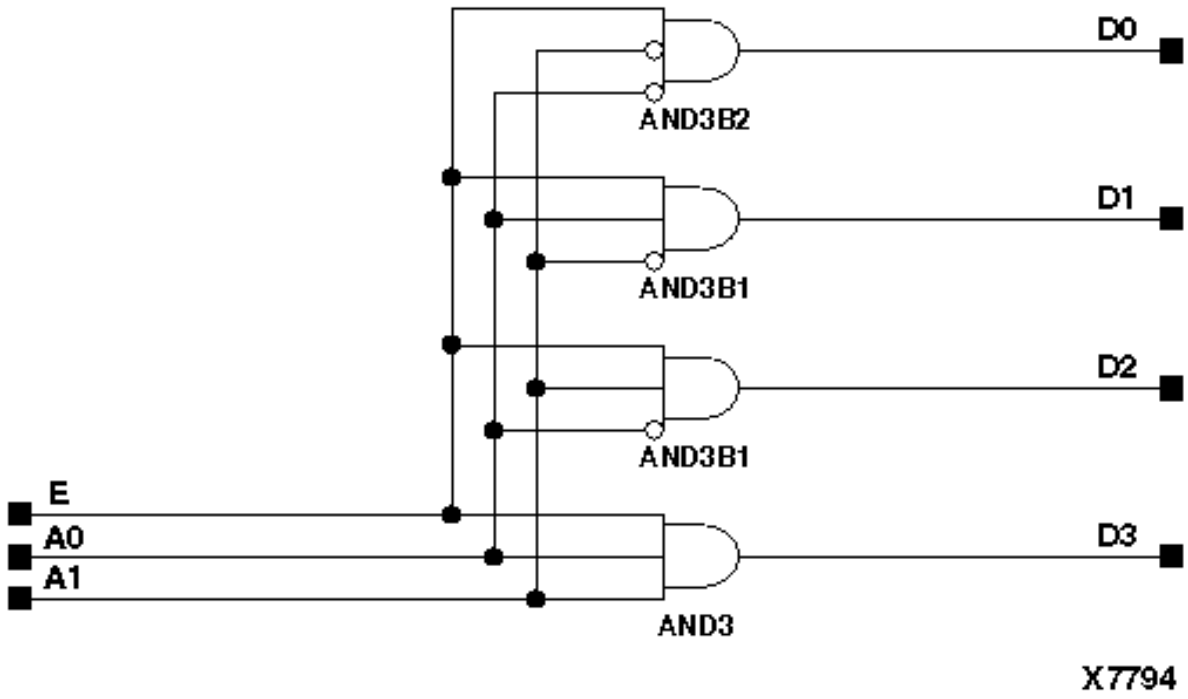
XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro



When the enable (EN) input of the D2_4E decoder/demultiplexer is High, one of four active-High outputs (D3 – D0) is selected with a 2-bit binary address (A1 – A0) input. The non-selected outputs are Low. Also, when the EN input is Low, all outputs are Low. In demultiplexer applications, the EN input is the data input.

Inputs			Outputs			
A1	**A0**	**E**	**D3**	**D2**	**D1**	**D0**
X	X	0	0	0	0	0
0	0	1	0	0	0	1
0	1	1	0	0	1	0
1	0	1	0	1	0	0
1	1	1	1	0	0	0

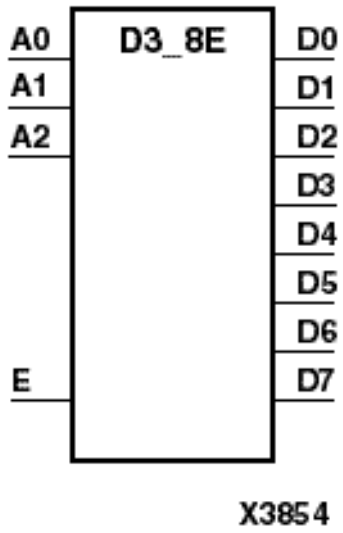
Figure 4-54D2_4E Implementation XC3000, XC4000, XC5200, XC9000, Spartans, Virtex



D3_8E

3- to 8-Line Decoder/Demultiplexer with Enable

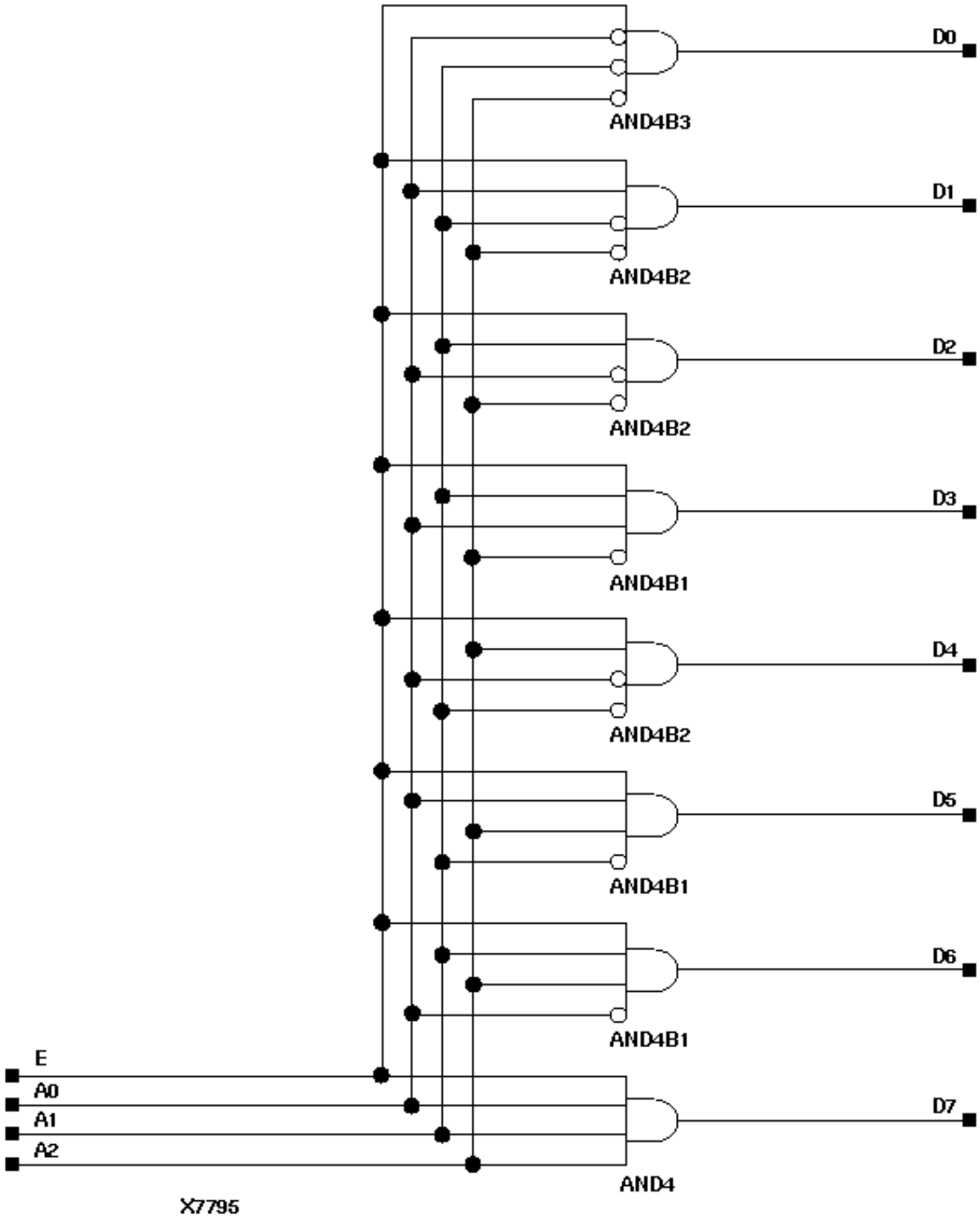
XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro



When the enable (EN) input of the D3_8E decoder/demultiplexer is High, one of eight active-High outputs (D7 – D0) is selected with a 3-bit binary address (A2 – A0) input. The non-selected outputs are Low. Also, when the EN input is Low, all outputs are Low. In demultiplexer applications, the EN input is the data input.

Inputs				Outputs							
A2	A1	A0	E	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0	1
0	0	1	1	0	0	0	0	0	0	1	0
0	1	0	1	0	0	0	0	0	1	0	0
0	1	1	1	0	0	0	0	1	0	0	0
1	0	0	1	0	0	0	1	0	0	0	0
1	0	1	1	0	0	1	0	0	0	0	0
1	1	0	1	0	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0

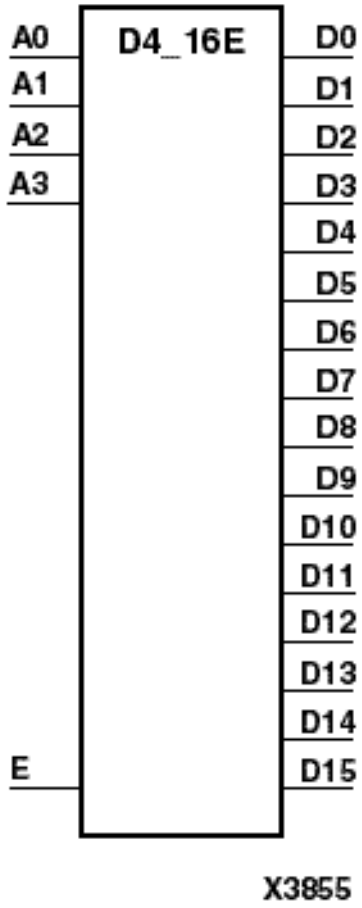
Figure 4-55D3_8E Implementation XC3000, XC4000, XC5200, XC9000, Spartans, Virtex



D4_16E

4- to 16-Line Decoder/Demultiplexer with Enable

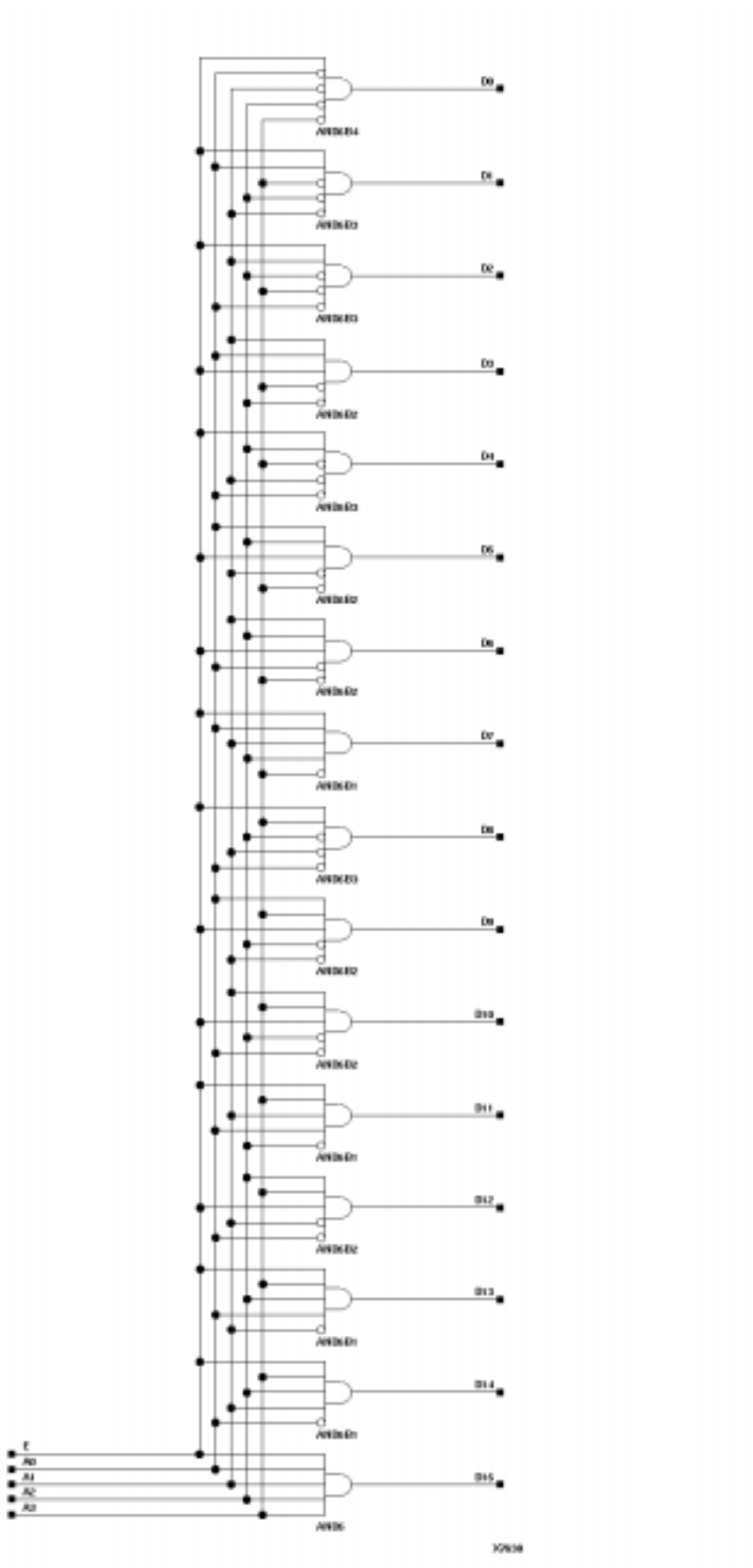
XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
Macro	Macro	Macro	Macro	Macro	Macro	Macro	Macro



When the enable (EN) input of the D4_16E decoder/demultiplexer is High, one of 16 active-High outputs (D15 – D0) is selected with a 4-bit binary address (A3 – A0) input. The non-selected outputs are Low. Also, when the EN input is Low, all outputs are Low. In demultiplexer applications, the EN input is the data input.

Refer to the **"D3_8E"** section for a representative truth table derivation.

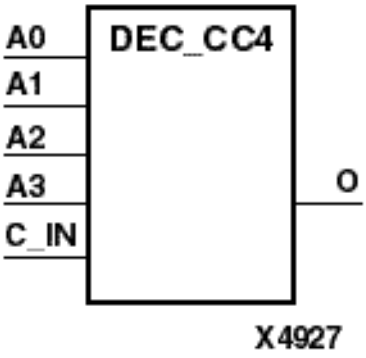
Figure 4-56D4_16E Implementation XC3000, XC4000, XC5200, XC9000, Spartans, Virtex



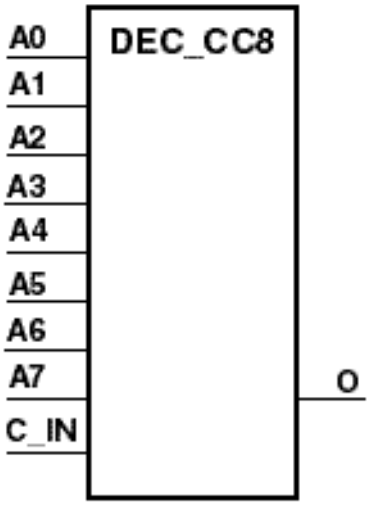
DEC_CC4, 8, 16

4-, 8-, 16-Bit Active Low Decoders

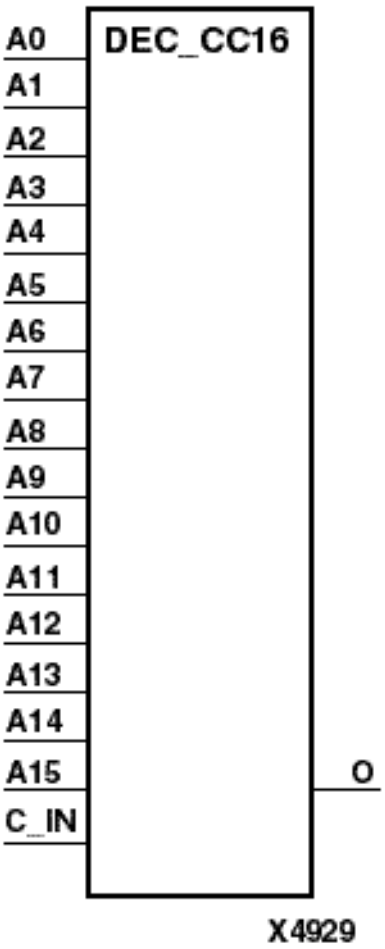
XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	N/A	Macro	N/A	N/A	N/A	Macro



X4927



X4928



These decoders are used to build wide-decoder functions. They are implemented by cascading CY_MUX elements driven by lookup tables (LUTs). The C_IN pin can only be driven by a CY_INIT or by the output (O) of a previous decode stage. When one or more of the inputs (A) are Low, the output is Low. When all the inputs are High and the C_IN input is High, the output is High. You can decode patterns by adding inverters to inputs.

Inputs					Outputs
A0	**A1**	**...**	**Az**	**C_IN**	**O**
1	1	1	1	1	1
X	X	X	X	0	0
0	X	X	X	X	0
X	0	X	X	X	0
X	X	X	0	X	0

z = 3 for DEC_CC4; z = 7 for DECC_CC8; z = 15 for

DECC_CC16

Figure 4-57DEC_CC4 Implementation XC5200

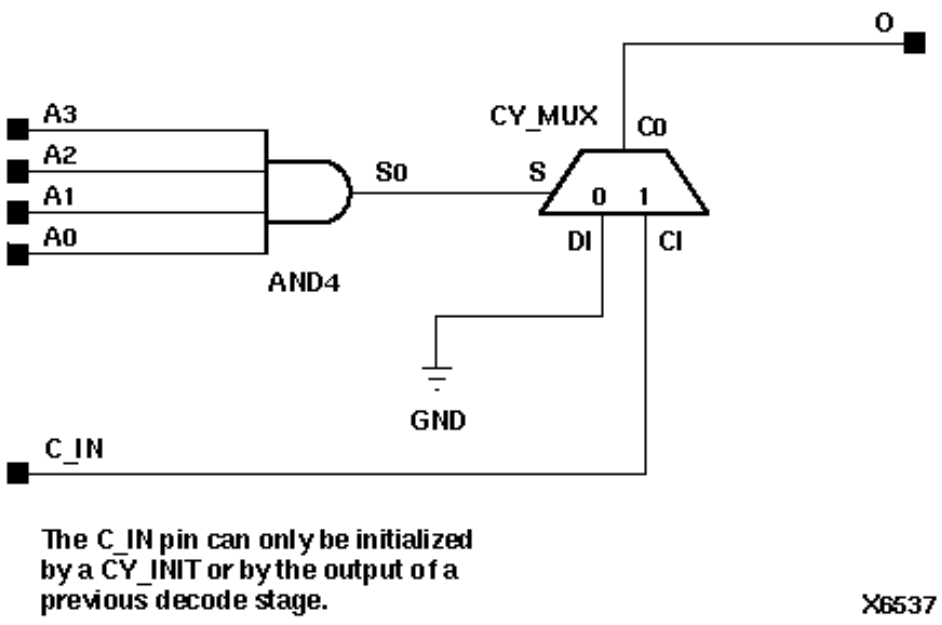


Figure 4-58DEC_CC4 Implementation Virtex

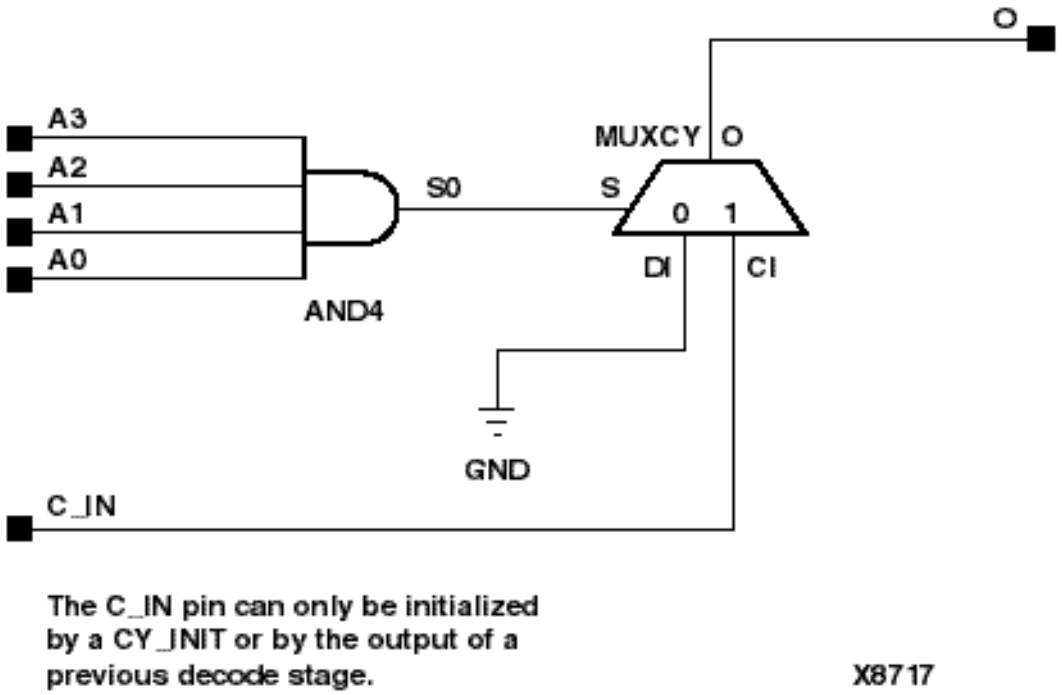
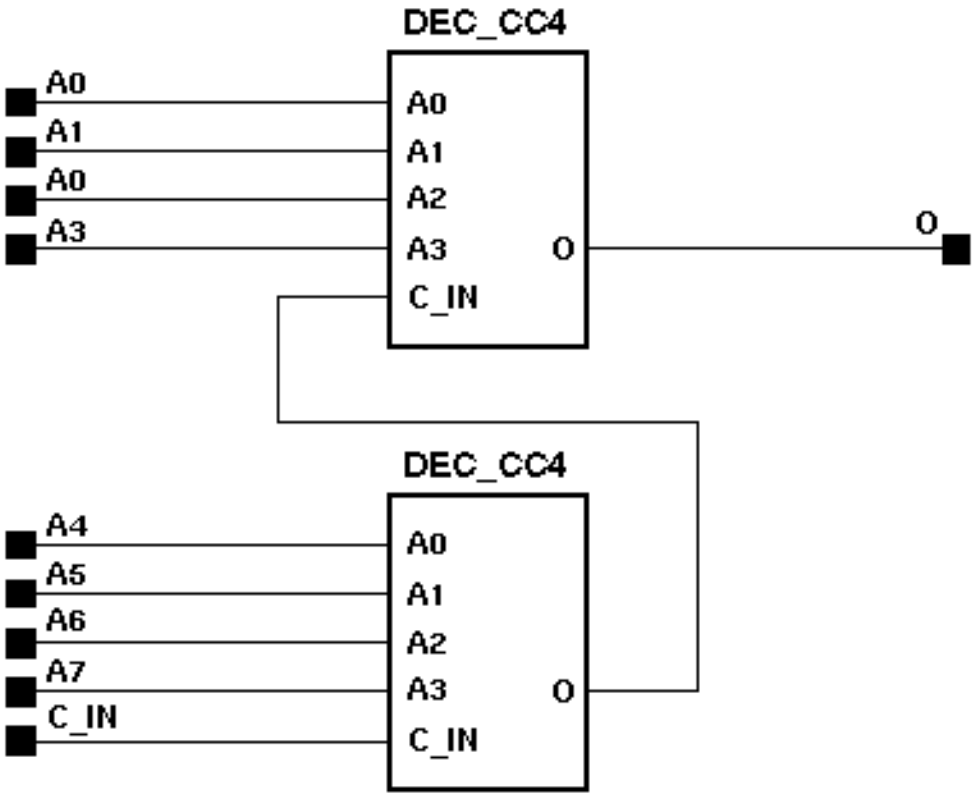


Figure 4-59DEC_CC8 Implementation XC5200, Virtex

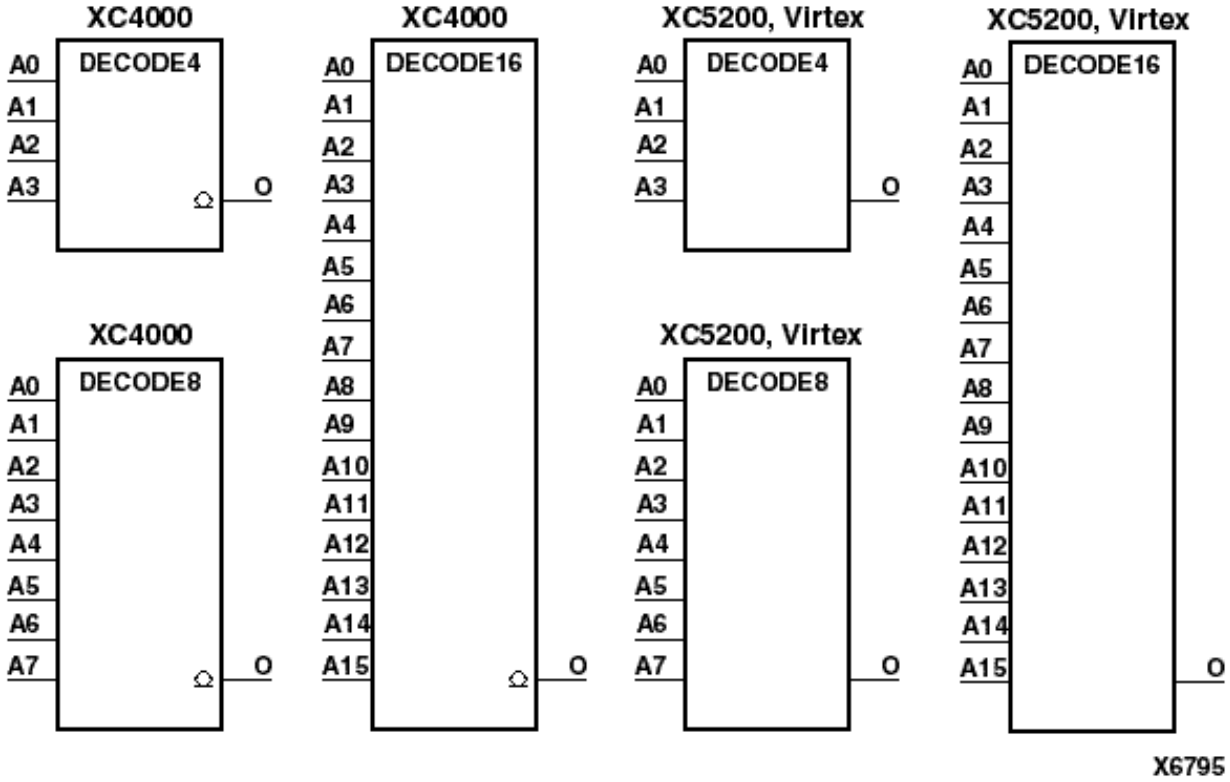


DECODE4, 8, 16

4-, 8-, 16-Bit Active-Low Decoders

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	Macro	Macro	Macro	N/A	N/A	N/A	Macro

Figure 4-60DECODE Representations



In the XC4000 architectures, decoders are open-drain, wired-AND gates. When one or more of the inputs (A) are Low, output (O) is Low. When all the inputs are High, the output is High or Off. A pull-up resistor must be connected to the output node to achieve a true logic High. A double pull-up resistor can be used to achieve faster performance; however, it uses more power. The software implements these macros using the open-drain AND gates around the periphery of the devices. (Diamonds in library symbols indicate an open-drain output.)

In XC5200, decoders are implemented by cascading CY_MUX elements driven by lookup tables (LUTs). When one or more of the inputs are Low, the output is Low. When all the inputs are High, the output is High. You can decode patterns by adding inverters to inputs. Pull-ups cannot be used on XC5200 longlines.

In Virtex, decoders are implemented using combinations of LUTs and MUXCYs.

Inputs				**Outputs***
A0	**A1**	**...**	**Az**	**O**
1	1	1	1	1
0	X	X	X	0
X	0	X	X	0
X	X	X	0	0

z = 3 for DECODE4, z = 7 for DECODE8; z = 15 for DECODE16
*A pull-up resistor must be connected to the output to establish
High-level drive current.

Figure 4-61DECODE8 Implementation XC4000

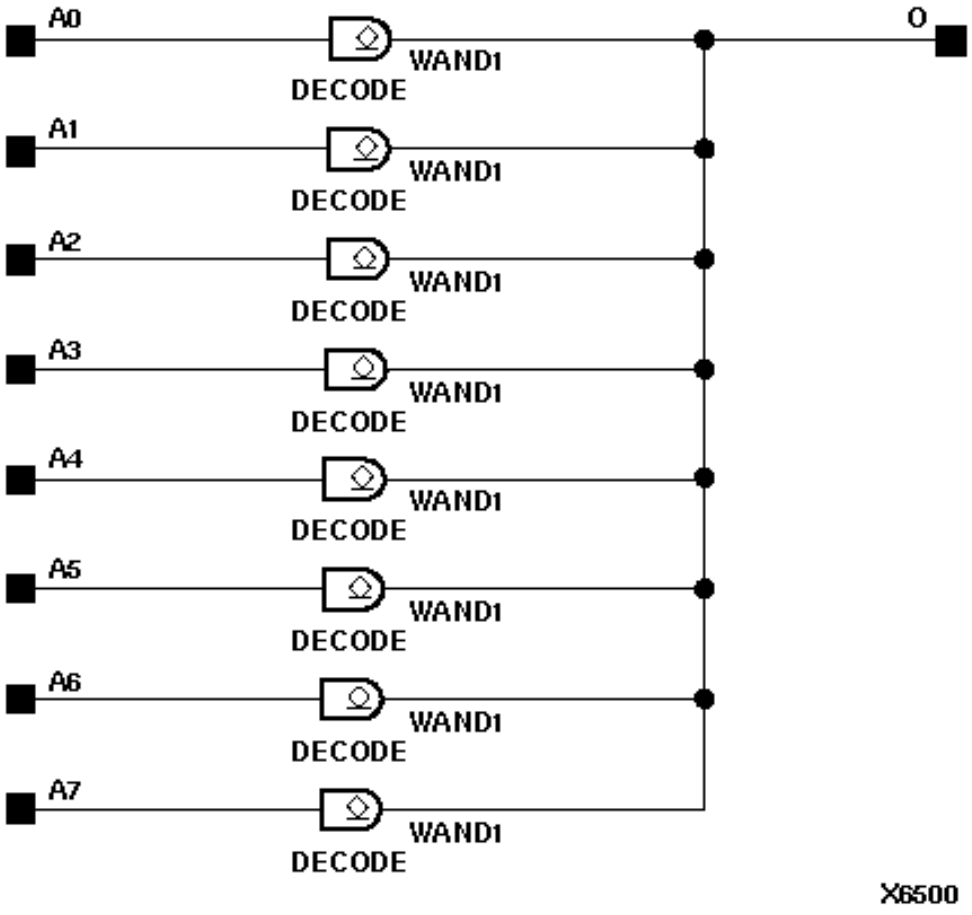


Figure 4-62DECODE8 Implementation XC5200

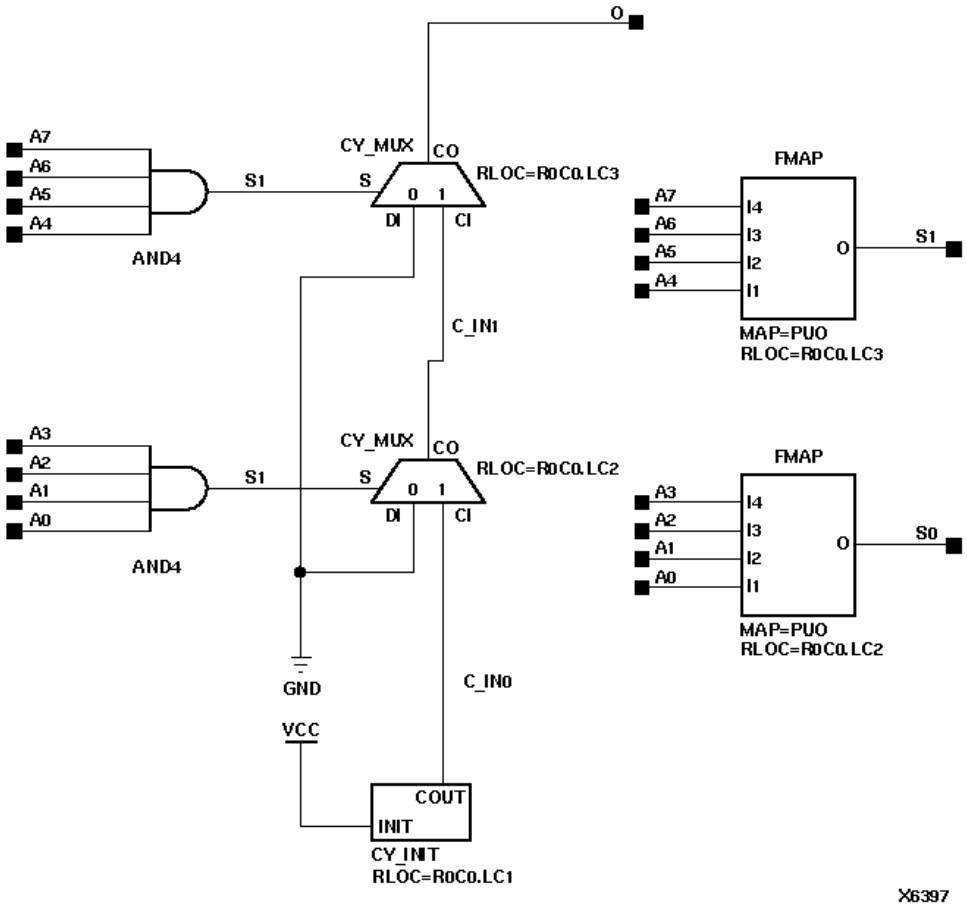
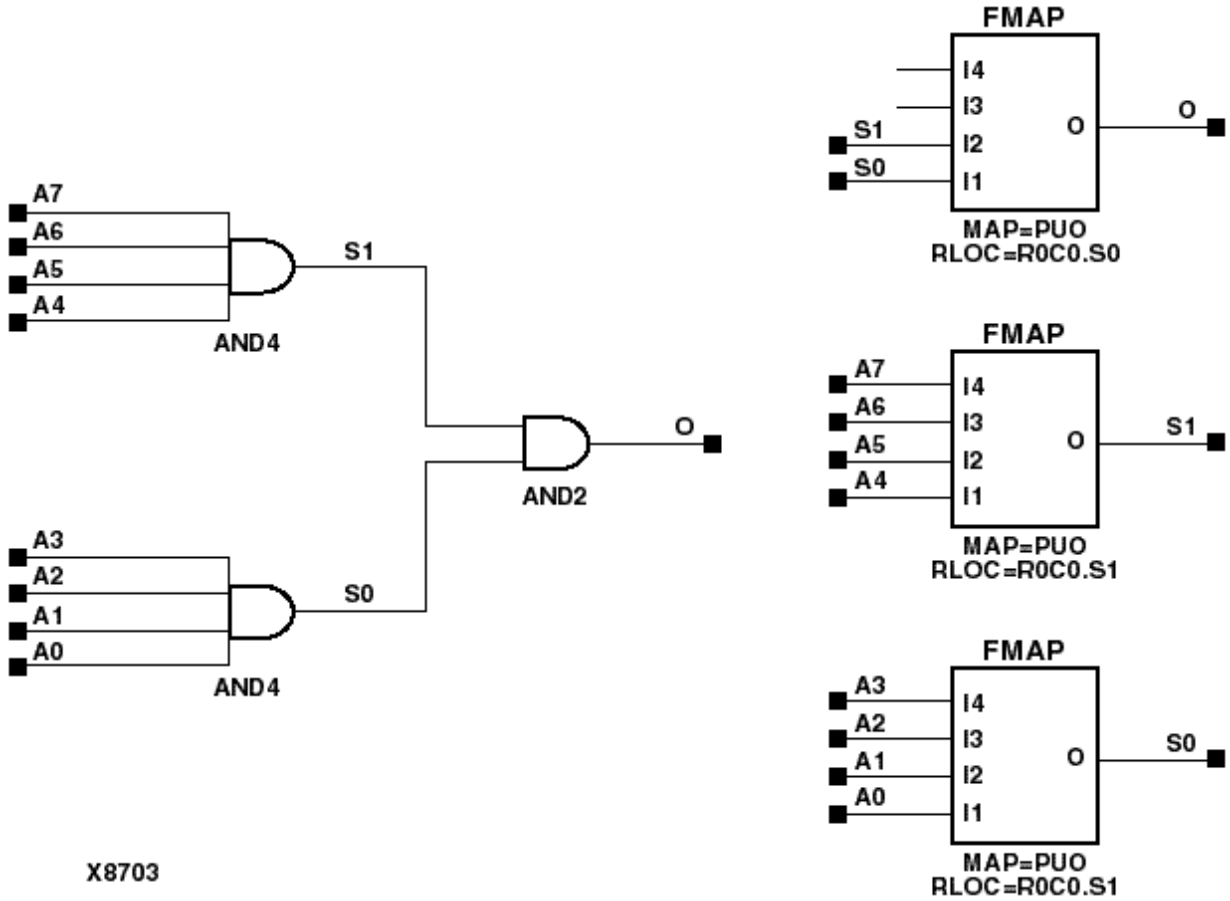


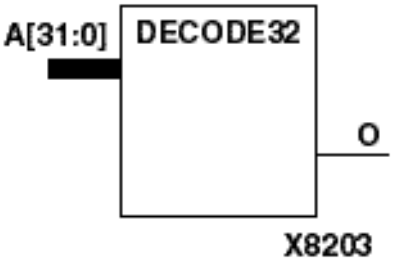
Figure 4-63DECODE8 Implementation Virtex



DECODE32, 64

32- and 64-Bit Active-Low Decoders

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
N/A	N/A	N/A	Macro	N/A	N/A	N/A	Macro



DECODE32 and DECODE64 are 32- and 64-bit active-low decoders. In XC5200, decoders are implemented by cascading CY_MUX elements driven by lookup tables (LUTs). When one or more of the inputs are Low, the output is Low. When all the inputs are High, the output is High. You can decode patterns by adding inverters to inputs. Pull-ups cannot be used on XC5200 longlines.

In Virtex, decoders are implemented using combinations of LUTs and MUXCYs.

Refer to the **"DECODE4, 8, 16"** section for a representative schematic.

Inputs				Outputs
A0	**A1**	**...**	**Az**	**O**
1	1	1	1	1
0	X	X	X	0
X	0	X	X	0
X	X	X	0	0

z = 31 for DECODE32; z = 63 for DECODE64