Chapter 2
Selection Guide

This chapter provides a CLB count for the design elements in each library plus a list of the Relationally Placed Modules (RPMs) by family. It also categorizes, by function, the logic elements that are described in detail in the "Design Elements" sections.

The chapter contains three major sections.

- **"CLB Count"**
- **"Relationally Placed Macros"**
- **"Functional Categories"**

CLB Count

Configurable Logic Blocks (CLBs) implement most of the logic in an FPGA. The following CLB Count table lists FPGA design elements in alphanumeric order with the number of CLBs needed for their implementation in each applicable library. Refer to the **"Applicable Architectures" section of the "Xilinx Unified Libraries" chapter** for information on the specific device architectures supported in each library.

Each XC5200 CLB contains four independent Logic Cells™ (LCs). In the following table, the numbers in the XC5200 column are the LC4 count.

Each Virtex CLB contains two slices. In the following table, the numbers in the Virtex column are the combined count for the two slices.

Note: This information is for reference only. The actual count could vary, depending upon the switch settings of the implementation tools; for example, the effort level in PAR (Place and Route).

Name	XC3000	XC4000E	XC4000X	XC5200*	Spartan	SpartanXL	Virtex**
ACC4	9	7	7	15	7	7	5
ACC8	17	11	11	27	11	11	9
ACC16	33	19	19	51	19	19	17
ACLK	1	-	-	-	-	-	-
ADD4	5	4	4	10	4	4	3
ADD8	9	6	6	18	6	6	5
ADD16	17	10	10	34	10	10	9
ADSU4	5	4	4	10	4	4	3
ADSU8	9	6	6	18	6	6	5

ADSU16	17	10	10	34	10	10	9
AND2	1	-	-	1	-	-	1
AND3	1	-	-	1	-	-	1
AND4	1	-	-	1	-	-	1
AND5	1	1	1	2	1	1	1
AND6	2	1	1	2	1	1	1
AND7	2	1	1	3	1	1	1
AND8	2	1	1	3	1	1	2
AND9	2	1	1	4	1	1	2
AND12	-	-	-	4	-	-	2
AND16	-	-	-	5	-	-	2
BRLSHFT4	4	4	4	4	4	4	8
BRLSHFT8	12	12	12	12	12	12	12
BSCAN	-	-	-	3	-	-	-
BUFE	1	-	-	-	-	-	-
BUFE4	1	-	-	-	-	-	-
BUFE8	1	-	-	-	-	-	-
BUFE16	1	-	-	-	-	-	-
BUFG	1	-	-	1	-	-	-
BUFGP	-	-	-	1	-	-	-
BUFGS	-	-	-	1	-	-	-
CB2CE	3	2	2	4	2	2	2
CB2CLE	4	3	3	5	3	3	3
CB2CLED	4	3	3	6	3	3	3
CB2RE	3	2	2	4	2	2	2
CB4CE	4	3	3	6	3	3	3
CB4CLE	7	5	5	9	5	5	5
CB4CLED	8	7	7	10	7	7	6
CB4RE	4	4	4	8	4	4	3
CB8CE	8	6	6	13	6	6	6
CB8CLE	13	10	10	18	10	10	9

CB8CLED	14	12	13	22	12	13	12
CB8RE	9	8	8	17	8	8	6
CB16CE	16	12	12	27	12	12	13
CB16CLE	26	18	18	36	18	18	18
CB16CLED	28	25	25	46	25	25	24
CB16RE	18	18	18	35	18	18	13
CC8CE	-	5	5	18	5	5	8
CC8CLE	-	6	6	19	6	6	9
CC8CLED	-	11	11	19	11	11	9
CC8RE	-	5	5	18	5	5	9
CC16CE	-	9	9	34	9	9	16
CC16CLE	-	10	10	35	10	10	17
CC16CLED	-	19	19	35	19	19	17
CC16RE	-	9	9	34	9	9	17
CD4CE	4	3	3	6	3	3	3
CD4CLE	7	5	5	10	5	5	5
CD4RE	5	6	5	9	6	5	3
CD4RLE	10	9	9	17	9	9	7
CJ4CE	2	2	2	4	2	2	2
CJ4RE	2	4	4	4	4	4	2
CJ5CE	3	3	3	5	3	3	3
CJ5RE	3	5	5	5	5	5	3
CJ8CE	4	4	4	8	4	4	4
CJ8RE	4	8	8	8	8	8	4
COMP2	1	1	1	1	1	1	1
COMP4	4	1	1	3	1	1	2
COMP8	9	4	4	5	4	4	3
COMP16	17	9	9	11	9	9	6
COMPM2	3	1	1	5	1	1	1
COMPM4	8	2	2	13	2	2	5

COMPM8	19	8	8	27	8	8	11
COMPM16	39	21	21	64	21	21	24
COMPMC8	-	7	7	18	7	7	8
COMPMC16	-	11	11	34	11	11	16
CR8CE	8	8	8	8	8	8	8
CR16CE	16	16	16	16	16	16	16
CY_INIT	-	-	-	1	-	-	-
CY_MUX	-	-	-	2	-	-	-
D2_4E	2	2	2	4	2	2	2
D3_8E	4	4	4	8	4	4	4
D4_16E	16	16	16	32	16	16	16
DEC_CC4	-	-	-	2	-	-	1
DEC_CC8	-	-	-	3	-	-	1
DEC_CC16	-	-	-	5	-	-	2
DECODE4	-	-	-	2	-	-	1
DECODE8	-	-	-	3	-	-	2
DECODE16	-	-	-	5	-	-	2
DECODE32	-	-	-	9	-	-	4
DECODE64	-	-	-	18	-	-	8
F5_MUX	-	-	-	1	-	-	-
F5MAP	-	-	-	1	-	-	-
FD	1	-	-	1	-	-	-
FD_1	1	-	-	1	-	-	-
FD4CE	4	2	2	4	2	2	2
FD4RE	2	4	4	4	4	4	2
FD8CE	4	4	4	8	4	4	4
FD8RE	4	8	8	8	8	8	4
FD16CE	8	8	8	16	8	8	8
FD16RE	8	16	16	16	16	16	8
FDC	1	1	1	1	1	1	-
FDC_1	1	1	1	1	1	1	-

FDCE	1	1	1	1	1	1	-
FDCE_1	1	1	1	1	1	1	-
FDP	-	1	1	1	1	1	-
FDP_1	-	1	1	1	1	1	-
FDPE	-	-	-	1	-	-	-
FDPE_1	-	1	1	1	1	1	-
FDR	1	1	1	1	1	1	-
FDRE	1	1	1	1	1	1	-
FDRS	1	1	1	1	1	1	-
FDRSE	1	2	2	3	2	2	-
FDS	1	1	1	1	1	1	-
FDSE	1	1	1	1	1	1	-
FDSR	1	1	1	1	1	1	-
FDSRE	1	2	2	3	2	2	-
FJKC	1	1	1	1	1	1	1
FJKCE	1	1	1	1	1	1	1
FJKP	-	1	1	1	1	1	1
FJKPE	-	1	1	1	1	1	1
FJKRSE	2	2	2	3	2	2	1
FJKSRE	2	2	2	3	2	2	1
FTC	1	1	1	1	1	1	1
FTCE	1	1	1	1	1	1	1
FTCLE	1	1	1	2	1	1	1
FTCLEX	-	-	-	-	-	-	1
FTP	-	1	1	1	1	1	1
FTPE	-	1	1	1	1	1	1
FTPLE	-	1	1	2	1	1	1
FTRSE	1	2	2	3	2	2	1
FTRSLE	3	2	2	4	2	2	2
FTSRE	1	2	2	3	2	2	1
FTSRLE	3	2	2	4	2	2	2

GCLK	1	-	-	-	-	-	-
IFD	-	-	-	1	-	-	-
IFD_1	-	-	-	1	-	-	-
IFD4	-	-	-	4	-	-	-
IFD8	-	-	-	8	-	-	-
IFD16	-	-	-	16	-	-	-
ILD	-	-	-	1	-	-	1
ILD_1	-	-	-	1	-	-	1
ILD4	-	-	-	4	-	-	2
ILD8	-	-	-	8	-	-	4
ILD16	-	-	-	16	-	-	8
IOPAD	-	-	-	1	-	-	-
LD	-	-	1	1	-	1	-
LD4	-	-	4	-	-	4	2
LD8	-	-	8	-	-	8	4
LD16	-	-	16	-	-	16	8
LD4CE	-	-	4	4	-	4	2
LD8CE	-	-	8	8	-	8	4
LD16CE	-	-	16	16	-	16	8
LD_1	-	-	1	1	-	1	-
LDC	-	-	1	1	-	1	-
LDC_1	-	-	1	1	-	1	-
LDCE	-	-	1	1	-	1	-
LDCE_1	-	-	-	1	-	-	-
LDPE	-	-	1	-	-	1	-
LDPE_1	-	-	1	-	-	1	-
M2_1	1	1	1	1	1	1	1
M2_1B1	1	1	1	1	1	1	1
M2_1B2	1	1	1	1	1	1	1
M2_1E	1	1	1	1	1	1	1
M4_1E	3	1	1	1	1	1	1

M8_1E	6	3	3	7	3	3	2
M16_1E	11	7	7	14	7	7	5
NAND2	1	-	-	1	-	-	1
NAND3	1	-	-	1	-	-	1
NAND4	1	-	-	1	-	-	1
NAND5	1	1	1	2	1	1	1
NAND6	2	1	1	2	1	1	1
NAND7	2	1	1	3	1	1	1
NAND8	2	1	1	3	1	1	2
NAND9	2	1	1	4	1	1	2
NAND12	-	-	-	4	-	-	2
NAND16	-	-	-	5	-	-	2
NOR2	1	-	-	1	-	-	1
NOR3	1	-	-	1	-	-	1
NOR4	1	-	-	1	-	-	1
NOR5	1	1	1	2	1	1	1
NOR6	2	1	1	2	1	1	1
NOR7	2	1	1	3	1	1	1
NOR8	2	1	1	3	1	1	2
NOR9	2	1	1	4	1	1	2
NOR12	-	-	-	4	-	-	2
NOR16	-	-	-	5	-	-	2
OFD	-	-	-	1	-	-	-
OFD_1	-	-	-	1	-	-	-
OFD4	-	-	-	4	-	-	-
OFD8	-	-	-	8	-	-	-
OFD16	-	-	-	16	-	-	-
OFDE	-	-	-	1	-	-	-
OFDE_1	-	-	-	1	-	-	-
OFDE4	-	-	-	4	-	-	-

OFDE8	-	-	-	8	-	-	-
OFDE16	-	-	-	16	-	-	-
OFDT	-	-	-	1	-	-	-
OFDT_1	-	-	-	1	-	-	-
OFDT4	-	-	-	4	-	-	-
OFDT8	-	-	-	8	-	-	-
OFDT16	-	-	-	16	-	-	-
OR2	1	-	-	1	-	-	1
OR3	1	-	-	1	-	-	1
OR4	1	-	-	1	-	-	1
OR5	1	1	1	2	1	1	1
OR6	2	1	1	2	1	1	1
OR7	2	1	1	3	1	1	1
OR8	2	1	1	3	1	1	2
OR9	2	1	1	3	1	1	2
OR12	-	-	-	4	-	-	2
OR16	-	-	-	5	-	-	2
RAM16X2	-	1	1	-	1	1	-
RAM16X2D	-	2	2	-	2	2	2
RAM16X2S	-	1	1	-	1	1	2
RAM16X4	-	2	2	-	2	2	-
RAM16X4D	-	4	4	-	4	4	4
RAM16X4S	-	2	2	-	2	2	4
RAM16X8	-	4	4	-	4	4	-
RAM16X8D	-	8	8	-	8	8	8
RAM16X8S	-	4	4	-	4	4	8
RAM32X2	-	2	2	-	2	2	-
RAM32X2S	-	2	-	-	2	-	2
RAM32X4	-	4	4	-	4	4	4
RAM32X4S	-	4	4	-	4	4	8
RAM32X8	-	8	8	-	8	8	-

RAM32X8S	-	8	8	-	8	8	-
SOP3	1	1	1	1	1	1	1
SOP4	1	1	1	1	1	1	1
SR4CE	2	2	2	4	2	2	2
SR4CLE	4	3	3	5	3	3	3
SR4CLED	5	5	5	10	5	5	5
SR4RE	2	4	4	4	4	4	2
SR4RLE	6	5	5	9	5	5	3
SR4RLED	7	8	8	14	8	8	5
SR8CE	4	4	4	8	4	4	4
SR8CLE	5	5	5	9	5	5	5
SR8CLED	9	9	9	18	9	9	9
SR8RE	4	8	8	8	8	8	4
SR8RLE	12	9	9	17	9	9	5
SR8RLED	13	9	9	26	9	9	9
SR16CE	8	8	8	16	8	8	8
SR16CLE	9	9	9	17	9	9	9
SR16CLED	17	17	17	34	17	17	17
SR16RE	8	16	16	16	16	16	8
SR16RLE	24	20	20	33	20	20	9
SR16RLED	25	19	19	50	19	19	17
UPAD	-	-	-	1	-	-	-
XNOR2	1	-	-	1	-	-	1
XNOR3	1	-	-	1	-	-	1
XNOR4	1	-	-	1	-	-	1
XNOR5	1	1	1	2	1	1	1
XNOR6	2	1	1	2	1	1	1
XNOR7	2	1	1	3	1	1	1
XNOR8	2	1	1	3	1	1	2
XNOR9	2	1	1	3	1	1	2
XOR2	1	-	-	1	-	-	1

XOR3	1	-	-	1	-	-	1
XOR4	1	-	-	1	-	-	1
XOR5	1	1	1	2	1	1	1
XOR6	2	1	1	2	1	1	1
XOR7	2	1	1	3	1	1	1
XOR8	2	1	1	3	1	1	2
XOR9	2	1	1	3	1	1	2
X74_42	5	5	5	10	5	5	-
X74_L85	14	9	9	20	9	9	-
X74_138	5	5	5	9	5	5	-
X74_139	2	2	2	4	2	2	-
X74_147	8	6	6	12	6	6	-
X74_148	10	6	6	14	6	6	-
X74_150	11	6	6	13	6	6	-
X74_151	6	3	3	7	3	3	-
X74_152	5	3	3	6	3	3	-
X74_153	6	3	3	6	3	3	-
X74_154	17	16	16	33	16	16	-
X74_157	4	2	2	4	2	2	-
X74_158	4	2	2	4	2	2	-
X74_160	8	6	6	11	6	6	-
X74_161	9	5	5	9	5	5	-
X74_162	8	6	6	13	6	6	-
X74_163	10	9	9	17	9	9	-
X74_164	5	4	4	8	4	4	-
X74_165S	8	5	5	9	5	5	-
X74_168	9	7	7	11	7	7	-
X74_174	7	4	4	6	4	4	-
X74_194	7	5	5	12	5	5	-
X74_195	5	3	3	5	3	3	-
X74_273	9	5	5	8	5	5	-

X74_280	3	2	2	5	2	2	-
X74_283	4	6	6	8	6	6	-
X74_298	4	2	2	4	2	2	-
X74_352	6	3	3	6	3	3	-
X74_377	9	4	4	8	4	4	-
X74_390	3	3	3	4	3	3	-
X74_518	9	4	4	6	4	4	-
X74_521	9	4	4	6	4	4	-

*LC4 count
**Combined count for the two Virtex slices
- = zero (0) or the component is not applicable for that architecture

Relationally Placed Macros

This section lists the Relationally Placed Macros (RPMs) by family. RPMs are "soft" macros that contain relative location constraint (RLOC) information. For more details, see the **"Relationally Placed Macros (RPMs)" section of the "Attributes, Constraints, and Carry Logic" chapter**.

The following table lists RPMs (except for CY4_* carry mode symbols) by library for easy identification. Refer to the **"Applicable Architectures" section of the "Xilinx Unified Libraries" chapter** for information on the specific device architectures supported in each library.

Note: The CY4_* RPMs are not listed here. To see a list of predefined carry mode names and their corresponding symbols (CY4_*), refer to the **"Carry Logic Primitives and Symbols" section of the "Attributes, Constraints, and Carry Logic" chapter**.

Element Name	XC4000 E	XC4000 X	XC5200	Spartan	Spartan XL	Virtex
ACC4	√	√	√	√	√	√
ACC8	√	√	√	√	√	√
ACC16	√	√	√	√	√	√
ADD4	√	√	√	√	√	√
ADD8	√	√	√	√	√	√
ADD16	√	√	√	√	√	√
ADSU4	√	√	√	√	√	√

ADSU8	√	√	√	√	√	√
ADSU16	√	√	√	√	√	√
AND6						√
AND7						√
AND8	√	√	√	√	√	√
AND9	√	√	√	√	√	√
AND12			√			√
AND16			√			√
CC8CE	√	√	√	√	√	√
CC8CLE	√	√	√	√	√	√
CC8CLED	√	√	√	√	√	√
CC8RE	√	√	√	√	√	√
CC16CE	√	√	√	√	√	√
CC16CLE	√	√	√	√	√	√
CC16CLED	√	√	√	√	√	√
CC16RE	√	√	√	√	√	√
COMPMC8	√	√	√	√	√	√
COMPMC16	√	√	√	√	√	√
CY_INIT			√			
CY_MUX			√			
DECODE4	√	√	√	√	√	√
DECODE8	√	√	√	√	√	√
DECODE16	√	√	√	√	√	√
DECODE32			√			√
DECODE64			√			√
DEC_CC4			√			
DEC_CC8			√			
DEC_CC16			√			

NAND6						√
NAND7						√
NAND8	√	√	√	√	√	√
NAND9	√	√	√	√	√	√
NAND12			√			√
NAND16			√			√
NOR6						√
NOR7						√
NOR8	√	√	√	√	√	√
NOR9	√	√	√	√	√	√
NOR12			√			√
NOR16			√			√
OR6						√
OR7						√
OR8						√
OR9						√
OR12			√			√
OR16			√			√
XNOR6						√
XNOR7						√
XNOR8						√
XNOR9						√
XOR6						√
XOR7						√
XOR8						√
XOR9						√

Functional Categories

This section categorizes, by function, the logic elements that are described in detail in the "Design Elements" sections. Each category is briefly described. Tables under each category identify all the available elements for the function and indicate which libraries include the element.

Elements are listed in alphanumeric order under each category. There are a number of standard TTL 7400-type functions in the different libraries. All 7400-type functions start with a "X74" prefix and are listed after all other elements. The numeric sequence following the "X74" prefix uses ascending numbers, for example, X74_42 precedes X74_138.

A check mark (√) in the column under the library name means that the element applies to the devices that use that library. (Refer to the **"Applicable Architectures" section of the "Xilinx Unified Libraries" chapter** for information on the specific device families that use each library.) A blank column means that the element does not apply.

The categories are as follows.

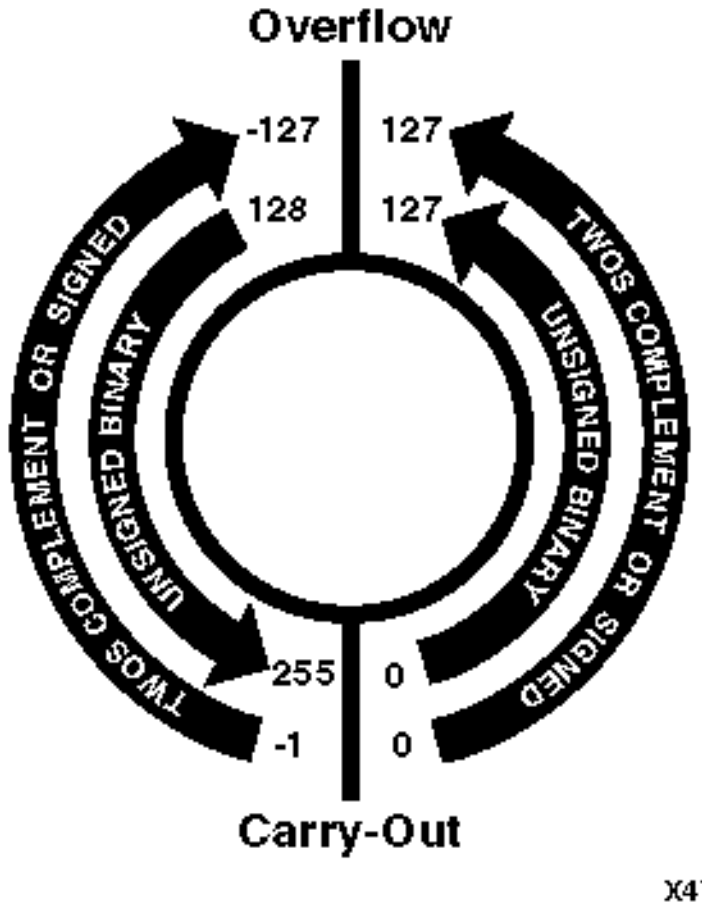
- **Arithmetic Functions**
- **Buffers**
- **Comparators**
- **Counters**
- **Data Registers**
- **Decoders**
- **Edge Decoders**
- **Encoders**
- **Flip-Flops**
- **General**
- **Input/Output Flip-Flops**
- **Input/Output Functions**
- **Input Latches**
- **Latches**
- **Logic Primitives**
- **Map Elements**
- **Memory Elements**
- **Multiplexers**
- **Shift Registers**
- **Shifters**

Note: When converting your design between FPGA families, use elements that have equivalent functions in each of the architectural families (libraries) to minimize re-designing.

Arithmetic Functions

There are three types of arithmetic functions: accumulators (ACC), adders (ADD), and adder/subtracters (ADSU). With an ADSU, either unsigned binary or twos-complement operations cause an overflow. If the result crosses the overflow boundary, an overflow is generated. Similarly, when the result crosses the carry-out boundary, a carry-out is generated. The following figure shows the ADSU carry-out and overflow boundaries.

Figure 2-1ADSU Carry-Out and Overflow Boundaries



ACC1		1-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
				√			

ACC4, 8, 16 4-, 8-, 16-Bit Loadable Cascadable Accumulators with Carry-In, Carry-Out, and Synchronous Reset

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	√

ADD1 1-Bit Full Adder with Carry-In and Carry-Out

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
				√			

ADD4, 8, 16 4-, 8-, 16-Bit Cascadable Full Adders with Carry-In, Carry-Out, and Overflow

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	√

ADSU1 1-Bit Cascadable Adder/Subtracter with Carry-In, Carry-Out

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
				√			

ADSU4, 8, 16 4-, 8-, 16-Bit Cascadable Adders/Subtracters with Carry-In, Carry-Out and Overflow

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	√

X74_280 9-Bit Odd/Even Parity Generator/Checker

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex

√	√	√	√	√	√	√	

X74_283		4-Bit Full Adder with Carry-In and Carry-Out					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√	√	√	√	

Buffers

The buffers in this section route high fan-out signals, 3-state signals, and clocks inside a PLD device. The **"Input/Output Functions" section** later in this chapter covers off-chip interface buffers.

ACLK		Alternate Clock Buffer					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√							

BUF		General-Purpose Buffer					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√	√	√	√	√

BUF4, 8, 16		General-Purpose Buffers					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
				√			

BUFCF		Fast Connect Buffer					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
							√

BUFE, 4, 8, 16 Internal 3-State Buffers with Active High Enable

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√*	√	√	√

* not supported for XC9500XL devices

BUFFCLK Global Fast Clock Buffer

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
		√					

BUFG Global Clock Buffer

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	√

BUFGDLL Clock Delay Locked Loop Buffer

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
							√

BUFGE Global Low Early Clock Buffer

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
		√					

BUFGLS Global Low Skew Clock Buffer

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
		√				√	

BUFGP		Primary Global Buffer for Driving Clocks or Longlines (Four per PLD Device)					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
	√		√		√		√

BUFGS		Secondary Global Buffer for Driving Clocks or Longlines (Four per PLD Device)					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
	√		√		√		

BUFGSR		Global Set/Reset Input Buffer					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
				√			

BUFGTS		Global Three-State Input Buffer					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
				√			

BUFOD		Open-Drain Buffer					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
	√	√					

BUFT, 4, 8, 16		Internal 3-State Buffers with Active-Low Enable					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**

√	√	√	√	√*	√	√	√

* not supported for XC9500XL devices

GCLK Global Clock Buffer

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√							

Comparators

There are two types of comparators, identity (COMP) and magnitude (COMPM).

COMP2, 4, 8, 16 2-, 4-, 8-, 16-Bit Identity Comparators

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	√

COMPM2, 4, 8, 16 2-, 4-, 8-, 16-Bit Magnitude Comparators

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	√

COMPMC8, 16 8-, 16-Bit Magnitude Comparators

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√	√		√	√	√

X74_L85 4-Bit Expandable Magnitude Comparator

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	

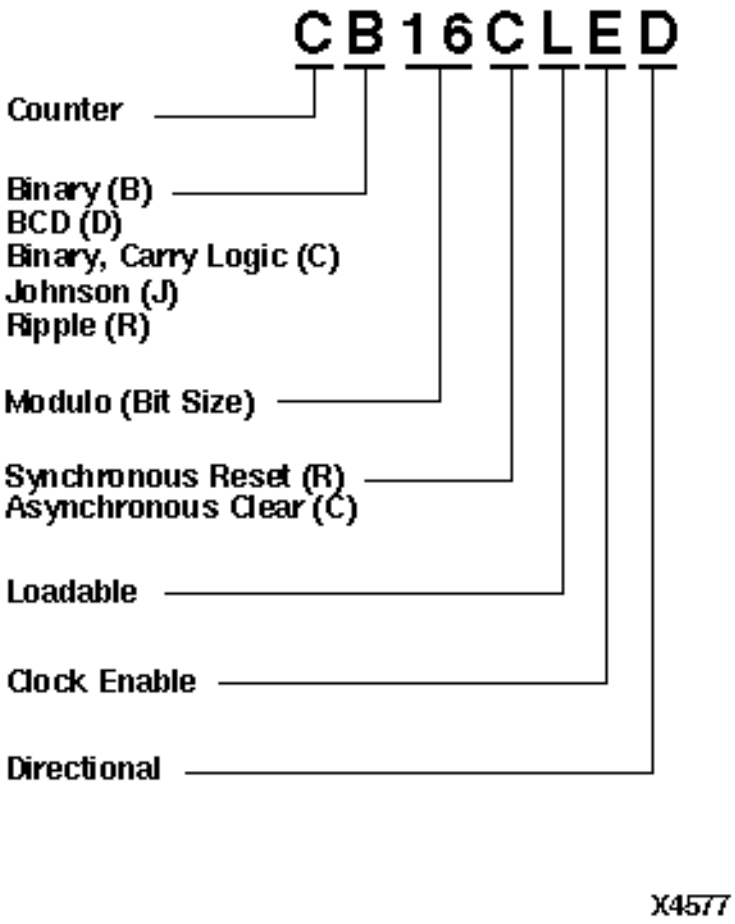
X74_518		8-Bit Identity Comparator with Active-Low Enable					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√	√	√	√	

X74_521		8-Bit Identity Comparator with Active-Low Enable and Output					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√	√	√	√	

Counters

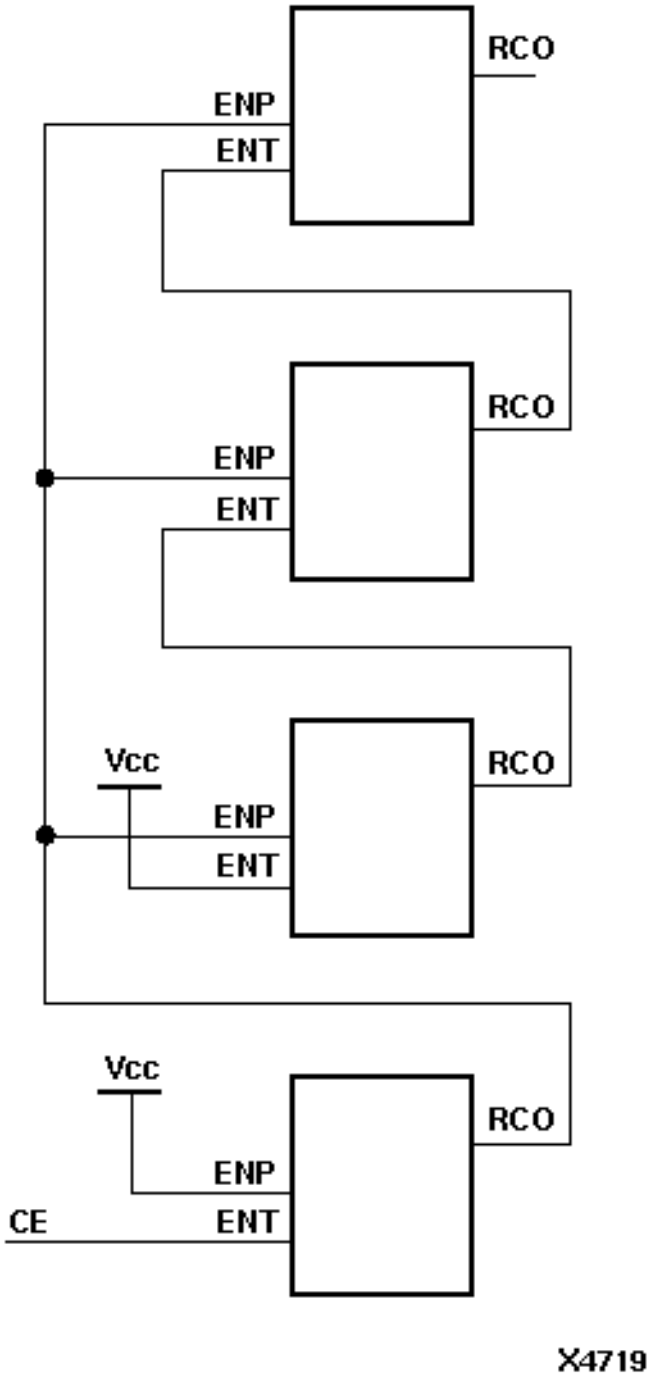
There are six types of counters with various synchronous and asynchronous inputs. The name of the counter defines the modulo or bit size, the counter type, and which control functions are included. The counter naming convention is shown in the following figure.

Figure 2-2Counter Naming Convention



A carry-lookahead design accommodates large counters without extra gating. On TTL 7400-type counters with trickle clock enable (ENT), parallel clock enable (ENP), and ripple carry-out (RCO), both the ENT and ENP inputs must be High to count. ENT is propagated forward to enable RCO, which produces a High output with the approximate duration of the QA output. The following figure illustrates a carry-lookahead design.

Figure 2-3Carry-Lookahead Design



The RCO output of the first stage of the ripple carry is connected to the ENP input of the second stage and all subsequent

stages. The RCO output of the second stage and all subsequent stages is connected to the ENT input of the next stage. The ENT of the second stage is always enabled/tied to VCC. CE is always connected to the ENT input of the first stage. This cascading method allows the first stage of the ripple carry to be built as a prescaler. In other words, the first stage is built to count very fast.

CB2CE, CB4CE, CB8CE, CB16CE	2-, 4-, 8-, 16-Bit Cascadable Binary Counters with Clock Enable and Asynchronous Clear

XC3000	**XC4000E**	**XC4000X**	**XC5200**	**XC9000**	**Spartan**	**SpartanXL**	**Virtex**
√	√	√	√	√	√	√	√

CB2CLE, CB4CLE, CB8CLE, CB16CLE	2-, 4-, 8-, 16-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear

XC3000	**XC4000E**	**XC4000X**	**XC5200**	**XC9000**	**Spartan**	**SpartanXL**	**Virtex**
√	√	√	√	√	√	√	√

CB2CLED, CB4CLED, CB8CLED, CB16CLED	2-, 4-, 8-, 16-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear

XC3000	**XC4000E**	**XC4000X**	**XC5200**	**XC9000**	**Spartan**	**SpartanXL**	**Virtex**
√	√	√	√	√	√	√	√

CB2RE, CB4RE, CB8RE, CB16RE	2-, 4-, 8-, 16-Bit Cascadable Binary Counters with Clock Enable and Synchronous Reset

XC3000	**XC4000E**	**XC4000X**	**XC5200**	**XC9000**	**Spartan**	**SpartanXL**	**Virtex**
√	√	√	√	√	√	√	√

CB2RLE, CB4RLE, CB8RLE,	2-, 4-, 8-, 16-Bit Loadable Cascadable Binary Counters with Clock Enable and Synchronous Reset

CB16RLE

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
				√			

CB2X1, CB4X1, CB8X1, CB16X1 2-, 4-, 8-, 16-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
				√			

CB2X2, CB4X2, CB8X2, CB16X2 2-, 4-, 8-, 16-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Synchronous Reset

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
				√			

CC8CE, CC16CE 8-, 16-Bit Cascadable Binary Counters with Clock Enable and Asynchronous Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√	√		√	√	√

CC8CLE, CC16CLE 8-, 16-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√	√		√	√	√

CC8CLED, CC16CLED 8-, 16-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear

XC3000	XC4000	XC4000	XC5200	XC9000	Spartan	Spartan	Virtex

	E	**X**				**XL**	
	√	√	√		√	√	√

CC8RE, CC16RE 8-, 16-Bit Cascadable Binary Counters with Clock Enable and Synchronous Reset

XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
	√	√	√		√	√	√

CD4CE 4-Bit Cascadable BCD Counter with Clock Enable and Asynchronous Clear

XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√	√	√	√	√

CD4CLE 4-Bit Loadable Cascadable BCD Counter with Clock Enable and Asynchronous Clear

XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√	√	√	√	√

CD4RE 4-Bit Cascadable BCD Counter with Clock Enable and Synchronous Reset

XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√	√	√	√	√

CD4RLE 4-Bit Loadable Cascadable BCD Counter with Clock Enable and Synchronous Reset

XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√	√	√	√	√

CJ4CE, CJ5CE, CJ8CE		4-, 5-, 8-Bit Johnson Counters with Clock Enable and Asynchronous Clear					
XC3000	**XC4000E**	**XC4000X**	**XC5200**	**XC9000**	**Spartan**	**SpartanXL**	**Virtex**
√	√	√	√	√	√	√	√

CJ4RE, CJ5RE, CJ8RE		4-, 5-, 8-Bit Johnson Counters with Clock Enable and Synchronous Reset					
XC3000	**XC4000E**	**XC4000X**	**XC5200**	**XC9000**	**Spartan**	**SpartanXL**	**Virtex**
√	√	√	√	√	√	√	√

CR8CE, CR16CE		8-, 16-Bit Negative-Edge Binary Ripple Counters with Clock Enable and Asynchronous Clear					
XC3000	**XC4000E**	**XC4000X**	**XC5200**	**XC9000**	**Spartan**	**SpartanXL**	**Virtex**
√	√	√	√	√	√	√	√

X74_160		4-Bit BCD Counter with Parallel and Trickle Enables, Active-Low Load Enable, and Asynchronous Clear					
XC3000	**XC4000E**	**XC4000X**	**XC5200**	**XC9000**	**Spartan**	**SpartanXL**	**Virtex**
√	√	√	√	√	√	√	

X74_161		4-Bit Binary Counter with Parallel and Trickle Enables, Active-Low Load Enable, and Asynchronous Clear					
XC3000	**XC4000E**	**XC4000X**	**XC5200**	**XC9000**	**Spartan**	**SpartanXL**	**Virtex**
√	√	√	√	√	√	√	

X74_162		4-Bit BCD Counter with Parallel and Trickle Enables, Active-Low Load Enable, and Synchronous Reset					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√	√	√	√	

X74_163		4-Bit Binary Counter with Parallel and Trickle Enables, Active-Low Load Enable, and Synchronous Reset					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√	√	√	√	

X74_168		4-Bit BCD Bidirectional Counter with Parallel and Trickle Clock Enables and Active-Low Load Enable					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√	√	√	√	

X74_390		4-Bit BCD/Bi-Quinary Ripple Counter with Negative-Edge Clocks and Asynchronous Clear					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√	√	√	√	

Data Registers

There are three TTL 7400-type data registers designed to function exactly as the TTL elements for which they are named.

X74_174		6-Bit Data Register with Active-Low Asynchronous Clear					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√	√	√	√	

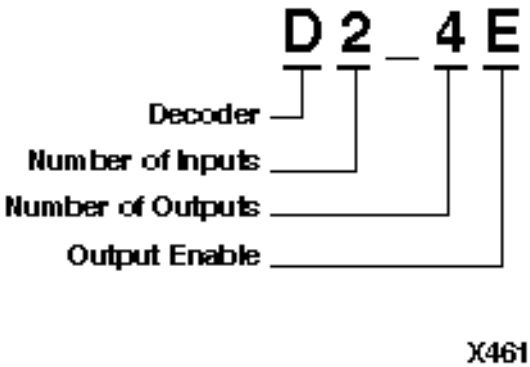
X74_273		8-Bit Data Register with Active-Low Asynchronous Clear					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√	√	√	√	

X74_377		8-Bit Data Register with Active-Low Clock Enable					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√	√	√	√	

Decoders

Decoder names, shown in the following figure, indicate the number of inputs and outputs and if an enable is available. Decoders with an enable can be used as multiplexers. This group includes some standard TTL 7400-type decoders whose names have an "X74" prefix.

Figure 2-4Decoder Naming Convention



D2_4E		2- to 4-Line Decoder/Demultiplexer with Enable					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√	√	√	√	√

D3_8E		3- to 8-Line Decoder/Demultiplexer with Enable					
XC3000	**XC4000**	**XC4000**	**XC5200**	**XC9000**	**Spartan**	**Spartan**	**Virtex**

	E	X				XL	
√	√	√	√	√	√	√	√

D4_16E 4- to 16-Line Decoder/Demultiplexer with Enable

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	√

DEC_CC4, 8, 16 4-, 8-, 16-Bit Active Low Decoders

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
			√				√

X74_42 4- to 10-Line BCD-to-Decimal Decoder with Active-Low Outputs

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	

X74_138 3- to 8-Line Decoder/Demultiplexer with Active-Low Outputs and Three Enables

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	

X74_139 2- to 4-Line Decoder/Demultiplexer with Active-Low Outputs and Active-Low Enable

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	

X74_154	4- to 16-Line Decoder/Demultiplexer with Two Enables and Active-Low Outputs

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	

Edge Decoders

Edge decoders are open-drain wired-AND gates that are available in different bit sizes.

DECODE4, 8, 16	4-, 8-, 16-Bit Active-Low Decoders

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√	√				√

DECODE32, 64	32- and 64-Bit Active-Low Decoders

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
			√				√

Encoders

There are two priority encoders (ENCPR) that function like the TTL 7400-type elements they are named after. There is a 10- to 4-line BCD encoder and an 8- to 3-line binary encoder.

X74_147	10- to 4-Line Priority Encoder with Active-Low Inputs and Outputs

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	

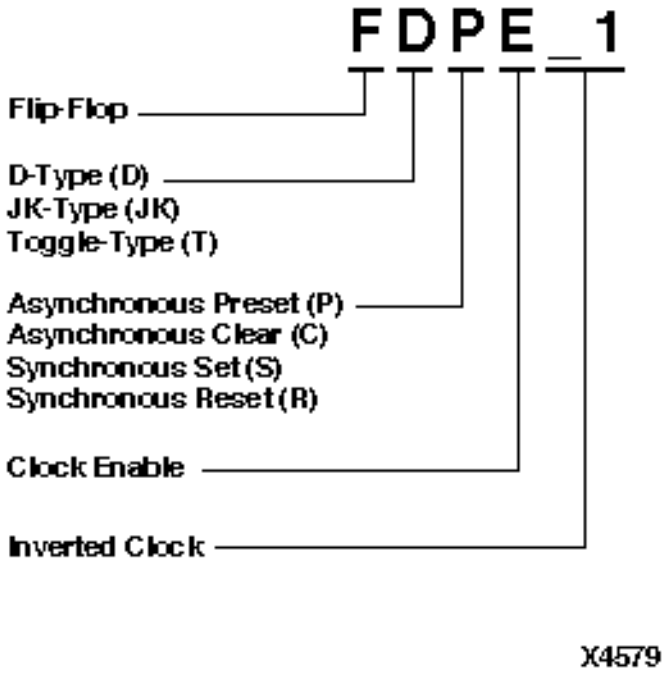
X74_148	8- to 3-Line Cascadable Priority Encoder with Active-Low Inputs and Outputs

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	

Flip-Flops

There are three types of flip-flops (D, J-K, toggle) with various synchronous and asynchronous inputs. Some are available with inverted clock inputs and/or the ability to set in response to global set/reset rather than reset. The naming convention shown in the following figure provides a description for each flip-flop. D-type flip-flops are available in multiples of up to 16 in one macro.

Figure 2-5Flip-Flop Naming Convention



FD		D Flip-Flop					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√	√	√	√	√

FD_1		D Flip-Flop with Negative-Edge Clock					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√		√	√	√

FD4, 8, 16 Multiple D Flip-Flops

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
				√			

FD4CE, FD8CE, FD16CE 4-, 8-, 16-Bit Data Registers with Clock Enable and Asynchronous Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	√

FD4RE, FD8RE, FD16RE 4-, 8-, 16-Bit Data Registers with Clock Enable and Synchronous Reset

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	√

FDC D Flip-Flop with Asynchronous Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	√

FDC_1 D Flip-Flop with Negative-Edge Clock and Asynchronous Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√		√	√	√

FDCE D Flip-Flop with Clock Enable and Asynchronous Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex

√	√	√	√	√	√	√	√

FDCE_1 D Flip-Flop with Negative-Edge Clock, Clock Enable, and Asynchronous Clear

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
√	√	√	√		√	√	√

FDCP D Flip-Flop with Asynchronous Preset and Clear

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
				√			√

FDCP_1 D Flip-Flop with Negative-Edge Clock and Asynchronous Preset and Clear

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
							√

FDCPE D Flip-Flop with Clock Enable and Asynchronous Preset and Clear

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
				√			√

FDCPE_1 D Flip-Flop with Negative-Edge Clock, Clock Enable, and Asynchronous Preset and Clear

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
							√

FDE D Flip-Flop with Clock Enable

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
							√

FDE_1 D Flip-Flop with Negative-Edge Clock and Clock Enable

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
							√

FDP D Flip-Flop with Asynchronous Preset

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√	√	√	√	√	√

FDP_1 D Flip-Flop with Negative-Edge Clock and Asynchronous Preset

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√	√		√	√	√

FDPE D Flip-Flop with Clock Enable and Asynchronous Preset

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√	√	√	√	√	√

FDPE_1 D Flip-Flop with Negative-Edge Clock, Clock Enable, and Asynchronous Preset

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√	√		√	√	√

FDR		D Flip-Flop with Synchronous Reset					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√	√	√	√	√

FDR_1		D Flip-Flop with Negative-Edge Clock and Synchronous Reset					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
							√

FDRE		D Flip-Flop with Clock Enable and Synchronous Reset					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√	√	√	√	√

FDRE_1		D Flip-Flop with Negative-Clock Edge, Clock Enable, and Synchronous Reset					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
							√

FDRS		D Flip-Flop with Synchronous Reset and Synchronous Set					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√	√	√	√	√

FDRS_1		D Flip-Flop with Negative-Clock Edge and Synchronous Reset and Set					
XC3000	**XC4000**	**XC4000**	**XC5200**	**XC9000**	**Spartan**	**Spartan**	**Virtex**

	E	X				XL	
							√

FDRSE D Flip-Flop with Synchronous Reset and Set and Clock Enable

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	√

FDRSE_1 D Flip-Flop with Negative-Clock Edge, Synchronous Reset and Set, and Clock Enable

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
							√

FDS D Flip-Flop with Synchronous Set

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	√

FDS_1 D Flip-Flop with Negative-Edge Clock and Synchronous Set

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
							√

FDSE D Flip-Flop with Clock Enable and Synchronous Set

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	√

FDSE_1 D Flip-Flop with Negative-Edge Clock, Clock Enable, and Synchronous Set

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
							√

FDSR D Flip-Flop with Synchronous Set and Reset

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	

FDSRE D Flip-Flop with Synchronous Set and Reset and Clock Enable

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	

FJKC J-K Flip-Flop with Asynchronous Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	√

FJKCE J-K Flip-Flop with Clock Enable and Asynchronous Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	√

FJKCP J-K Flip-Flop with Asynchronous Clear and Preset

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
				√			

FJKCPE		J-K Flip-Flop with Asynchronous Clear and Preset and Clock Enable					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
				√			

FJKP		J-K Flip-Flop with Asynchronous Preset					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
	√	√	√	√	√	√	√

FJKPE		J-K Flip-Flop with Clock Enable and Asynchronous Preset					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
	√	√	√	√	√	√	√

FJKRSE		J-K Flip-Flop with Clock Enable and Synchronous Reset and Set					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√	√	√	√	√

FJKSRE		J-K Flip-Flop with Clock Enable and Synchronous Set and Reset					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√	√	√	√	√

FTC		Toggle Flip-Flop with Toggle Enable and Asynchronous Clear					

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	√

FTCE Toggle Flip-Flop with Toggle and Clock Enable and Asynchronous Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	√

FTCLE Toggle/Loadable Flip-Flop with Toggle and Clock Enable and Asynchronous Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	√

FTCLEX Toggle/Loadable Flip-Flop with Toggle and Clock Enable and Asynchronous Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√	√		√	√	√

FTCP Toggle Flip-Flop with Toggle Enable and Asynchronous Clear and Preset

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
				√			

FTCPE Toggle Flip-Flop with Toggle and Clock Enable and Asynchronous Clear and Preset

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex

				√			

FTCPLE Loadable Toggle Flip-Flop with Toggle and Clock Enable and Asynchronous Clear and Preset

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	Spartan XL	Virtex
				√			

FTP Toggle Flip-Flop with Toggle Enable and Asynchronous Preset

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√	√	√	√	√	√

FTPE Toggle Flip-Flop with Toggle and Clock Enable and Asynchronous Preset

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√	√	√	√	√	√

FTPLE Toggle/Loadable Flip-Flop with Toggle and Clock Enable and Asynchronous Preset

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√	√	√	√	√	√

FTRSE Toggle Flip-Flop with Toggle and Clock Enable and Synchronous Reset and Set

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	√

FTRSLE		Toggle/Loadable Flip-Flop with Toggle and Clock Enable and Synchronous Reset and Set					
XC3000	**XC4000E**	**XC4000X**	**XC5200**	**XC9000**	**Spartan**	**SpartanXL**	**Virtex**
√	√	√	√	√	√	√	√

FTSRE		Toggle Flip-Flop with Toggle and Clock Enable and Synchronous Set and Reset					
XC3000	**XC4000E**	**XC4000X**	**XC5200**	**XC9000**	**Spartan**	**SpartanXL**	**Virtex**
√	√	√	√	√	√	√	√

FTSRLE		Toggle/Loadable Flip-Flop with Toggle and Clock Enable and Synchronous Set and Reset					
XC3000	**XC4000E**	**XC4000X**	**XC5200**	**XC9000**	**Spartan**	**SpartanXL**	**Virtex**
√	√	√	√	√	√	√	√

General

General elements include FPGA configuration functions, oscillators, boundary scan logic, and other functions not classified in other sections.

BSCAN		Boundary Scan Logic Control Circuit					
XC3000	**XC4000E**	**XC4000X**	**XC5200**	**XC9000**	**Spartan**	**SpartanXL**	**Virtex**
	√	√	√		√	√	

BSCAN_VIRTEX		Virtex Boundary Scan Logic Control Circuit					
XC3000	**XC4000E**	**XC4000X**	**XC5200**	**XC9000**	**Spartan**	**SpartanXL**	**Virtex**
							√

BYPOSC Bypass Oscillator

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
			√				

CAPTURE_VIRTEX Virtex Register State Capture for Bitstream Readback

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
							√

CK_DIV Internal Multiple-Frequency Clock Divider

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
			√				

CLB CLB Configuration Symbol

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
√							

CLKDLL Clock Delay Locked Loop

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
							√

CLKDLLHF High Frequency Clock Delay Locked Loop

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
							√

CONFIG Repository for Schematic-Level (Global) Attributes

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	√

CY_INIT Initialization Stage for Carry Chain

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
			√				

GND Ground-Connection Signal Tag

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	√

GXTL Crystal Oscillator with ACLK Buffer

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√							

IOB IOB Configuration Symbol

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√							

KEEPER KEEPER Symbol

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
							√

LUT1, 2, 3, 4		1-, 2-, 3-, 4-Bit Look-Up-Table with General Output					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
							√

LUT1_D, LUT2_D, LUT3_D, LUT4_D		1-, 2-, 3-, 4-Bit Look-Up-Table with Dual Output					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
							√

LUT1_L, LUT2_L, LUT3_L, LUT4_L		1-, 2-, 3-, 4-Bit Look-Up-Table with Local Output					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
							√

MD0		Mode 0, Input Pad Used for Readback Trigger Input					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
	√	√	√				

MD1		Mode 1, Output Pad Used for Readback Data Output					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
	√	√	√				

MD2		Mode 2, Input Pad					
XC3000	**XC4000**	**XC4000**	**XC5200**	**XC9000**	**Spartan**	**Spartan**	**Virtex**

	E	X				XL	
	√	√	√				

OSC Crystal Oscillator Amplifier

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√							

OSC4 Internal 5-Frequency Clock-Signal Generator

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√			√	√	

OSC5 Internal Multiple-Frequency Clock-Signal Generator

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
			√				

OSC52 Internal Multiple-Frequency Clock-Signal Generator

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
			√				

PULLDOWN Resistor to GND for Input Pads

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√	√		√	√	√

PULLUP Resistor to VCC for Input PADs, Open-Drain, and 3-State Outputs

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√		√	√	√

READBACK FPGA Bitstream Readback Controller

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√	√		√	√	

STARTUP User Interface to Global Clock, Reset, and 3-State Controls

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√	√		√	√	

STARTUP_VIRTEX Virtex User Interface to Global Clock, Reset, and 3-State Controls

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
							√

TCK Boundary Scan Test Clock Input Pad

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√	√		√	√	

TDI Boundary Scan Test Data Input Pad

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√	√		√	√	

TDO		Boundary Scan Data Output Pad					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
	√	√	√		√	√	

TIMEGRP		Schematic-Level Table of Basic Timing Specification Groups					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√	√	√	√	√

TIMESPEC		Schematic-Level Timing Requirement Table					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√	√	√	√	√

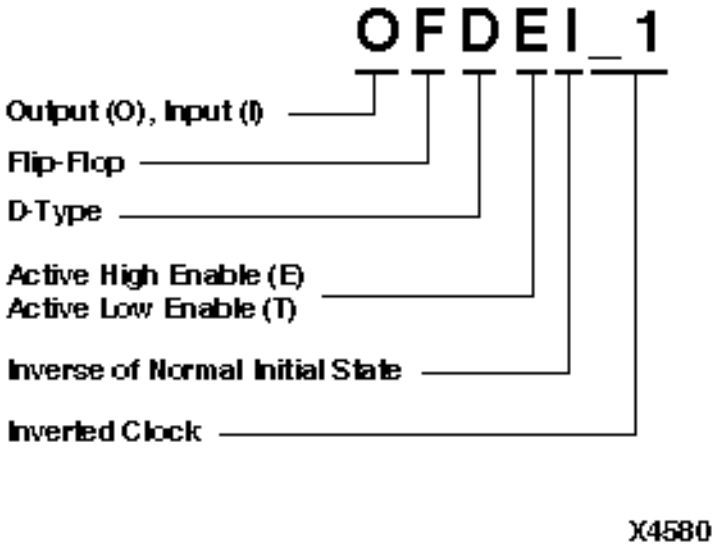
TMS		Boundary Scan Test Mode Select Input Pad					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
	√	√	√		√	√	

VCC		VCC-Connection Signal Tag					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√	√	√	√	√

Input/Output Flip-Flops

Input/Output flip-flops are configured in IOBs. They include flip-flops whose outputs are enabled by 3-state buffers, flip-flops that can be set upon global set/reset rather than reset, and flip-flops with inverted clock inputs. The naming convention specifies each flip-flop function and is illustrated in the following figure.

Figure 2-6Input/Output Flip-Flop Naming Convention



IFD, 4, 8, 16		Single- and Multiple-Input D Flip-Flops					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√	√	√	√	√

IFD_1		Input D Flip-Flop with Inverted Clock					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√		√	√	√

IFDI		Input D Flip-Flop (Asynchronous Preset)					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
	√	√			√	√	√

IFDI_1	Input D Flip-Flop with Inverted Clock (Asynchronous Preset)

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√			√	√	√

IFDX, 4, 8, 16 Single- and Multiple-Input D Flip-Flops with Clock Enable

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√			√	√	√

IFDX_1 Input D Flip-Flop with Inverted Clock and Clock Enable

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√			√	√	√

IFDXI Input D Flip-Flop with Clock Enable (Asynchronous Preset)

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√			√	√	√

IFDXI_1 Input D Flip-Flop with Inverted Clock and Clock Enable (Asynchronous Preset)

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√			√	√	√

OFD, 4, 8, 16 Single- and Multiple-Output D Flip-Flops

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	√

OFD_1		Output D Flip-Flop with Inverted Clock					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√		√	√	√

OFDE, 4, 8, 16		D Flip-Flops with Active-High Enable Output Buffers					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√	√	√	√	√

OFDE_1		D Flip-Flop with Active-High Enable Output Buffer and Inverted Clock					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√		√	√	√

OFDEI		D Flip-Flop with Active-High Enable Output Buffer (Asynchronous Preset)					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
	√	√			√	√	

OFDEI_1		D Flip-Flop with Active-High Enable Output Buffer and Inverted Clock (Asynchronous Preset)					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
	√	√			√	√	

OFDEX, 4, 8, 16	D Flip-Flops with Active-High Enable Output Buffers and Clock Enable

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√			√	√	

OFDEX_1 D Flip-Flop with Active-High Enable Output Buffer, Inverted Clock, and Clock Enable

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√			√	√	

OFDEXI D Flip-Flop with Active-High Enable Output Buffer and Clock Enable (Asynchronous Preset)

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√			√	√	

OFDEXI_1 D Flip-Flop with Active-High Enable Output Buffer, Inverted Clock, and Clock Enable (Asynchronous Preset)

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√			√	√	

OFDI Output D Flip-Flop (Asynchronous Preset)

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√			√	√	√

OFDI_1 Output D Flip-Flop with Inverted Clock (Asynchronous Preset)

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√			√	√	√

OFDT, 4, 8, 16		Single and Multiple D Flip-Flops with Active-Low 3-State Output Buffers					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√	√	√	√	√

OFDT_1		D Flip-Flop with Active-Low 3-State Output Buffer and Inverted Clock					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√		√	√	√

OFDTI		D Flip-Flop with Active-Low 3-State Output Buffer (Asynchronous Preset)					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
	√	√			√	√	

OFDTI_1		D Flip-Flop with Active-Low 3-State Output Buffer and Inverted Clock (Asynchronous Preset)					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
	√	√			√	√	

OFDTX, 4, 8, 16		Single and Multiple D Flip-Flops with Active-Low 3-State Output Buffers and Clock Enable					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
	√	√			√	√	

OFDTX_1 D Flip-Flop with Active-Low 3-State Output Buffer, Inverted Clock, and Clock Enable

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
	√	√			√	√	

OFDTXI D Flip-Flop with Active-Low 3-State Output Buffer and Clock Enable (Asynchronous Preset)

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
	√	√			√	√	

OFDTXI_1 D Flip-Flop with Active-Low 3-State Output Buffer, Inverted Clock, and Clock Enable (Asynchronous Preset)

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
	√	√			√	√	

OFDX, 4, 8, 16 Single- and Multiple-Output D Flip-Flops with Clock Enable

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
	√	√			√	√	√

OFDX_1 Output D Flip-Flop with Inverted Clock and Clock Enable

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
	√	√			√	√	√

OFDXI Output D Flip-Flop with Clock Enable (Asynchronous Preset)

XC3000	XC4000	XC4000	XC5200	XC9000	Spartan	Spartan	Virtex

	E	X				XL	
	√	√			√	√	√

OFDXI_1		Output D Flip-Flop with Inverted Clock and Clock Enable (Asynchronous Preset)					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
	√	√			√	√	√

Input/Output Functions

Input/Output Block (IOB) resources are configured into various I/O primitives and macros for convenience, such as, output buffers (OBUFs) and output buffers with an enable (OBUFEs). Pads used to connect the circuit to PLD device pins are also included.

Virtex has multiple variants (primitives) to choose from for each selectI/O buffer. The I/O interface for each variant corresponds to a specific I/O standard.

IBUF, 4, 8, 16		Single- and Multiple-Input Buffers					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√	√	√	√	√

IBUF_selectIO		Single Input Buffer with Selectable I/O Interface (16 primitives)					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
							√

IBUFG_selectIO		Dedicated Input Buffer with Selectable I/O Interface (16 primitives)					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
							√

IOBUF_selectIO Bi-Directional Buffer with Selectable I/0 Interface (30 primitives)

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
							√

IOPAD, 4, 8, 16 Single- and Multiple-Input/Output Pads

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	√

IPAD, 4, 8, 16 Single- and Multiple-Input Pads

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	√

OBUF, 4, 8, 16 Single- and Multiple-Output Buffers

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	√

OBUF_selectIO Single Output Buffer with Selectable I/O Interface (30 primitives)

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
							√

OBUFE, 4, 8, 16 3-State Output Buffers with Active-High Output Enable

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	√

OBUFT, 4, 8, 16	Single and Multiple 3-State Output Buffers with Active Low Output Enable						
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√	√	√	√	√

OBUFT_selectIO	Single 3-State Output Buffer with Active-Low Output Enable and Selectable I/O Interface (30 primitives)						
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
							√

OPAD, 4, 8, 16	Single- and Multiple-Output Pads						
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√	√	√	√	√

UPAD	Connects the I/O Node of an IOB to the Internal PLD Circuit						
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√		√	√	√

Input Latches

Single and multiple input latches can hold transient data entering a chip. Input latches use the same naming convention as I/O flip-flops.

ILD, 4, 8, 16	Transparent Input Data Latches						
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√	√	√	√	√

ILD_1		Transparent Input Data Latch with Inverted Gate					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√		√	√	√

ILDI		Transparent Input Data Latch (Asynchronous Preset)					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
	√	√			√	√	√

ILDI_1		Transparent Input Data Latch with Inverted Gate (Asynchronous Preset)					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
	√	√			√	√	√

ILDX, 4, 8, 16		Transparent Input Data Latches					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
	√	√			√	√	√

ILDX_1		Transparent Input Data Latch with Inverted Gate					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
	√	√			√	√	√

ILDXI		Transparent Input Data Latch (Asynchronous Preset)					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
	√	√			√	√	√

ILDXI_1		Transparent Input Data Latch with Inverted Gate (Asynchronous Preset)					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
	√	√			√	√	√

ILFFX		Fast Capture Input Latch					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
		√				√	

ILFFXI		Fast Capture Input Latch (Asynchronous Preset)					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
		√				√	

ILFLX		Fast Capture Transparent Input Latch					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
		√				√	

ILFLX_1		Fast Capture Input Latch with Inverted Gate					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
		√				√	

ILFLXI_1		Fast Capture Input Latch with Inverted Gate (Asynchronous Preset)					
XC3000	**XC4000**	**XC4000**	**XC5200**	**XC9000**	**Spartan**	**Spartan**	**Virtex**

E	X	XL
	√	√

Latches

Latches (LD) are only available in the XC4000X, XC5200, XC9000, SpartanXL, and Virtex architectures. XC3000 and XC4000E latches that existed in previous macro libraries are not recommended for new designs.

LD		Transparent Data Latch					
XC3000	**XC4000E**	**XC4000X**	**XC5200**	**XC9000**	**Spartan**	**SpartanXL**	**Virtex**
		√	√	√		√	√

LD_1		Transparent Data Latch with Inverted Gate					
XC3000	**XC4000E**	**XC4000X**	**XC5200**	**XC9000**	**Spartan**	**SpartanXL**	**Virtex**
		√	√			√	√

LD4, 8, 16		Multiple Transparent Data Latches					
XC3000	**XC4000E**	**XC4000X**	**XC5200**	**XC9000**	**Spartan**	**SpartanXL**	**Virtex**
		√		√		√	√

LDC		Transparent Data Latch with Asynchronous Clear					
XC3000	**XC4000E**	**XC4000X**	**XC5200**	**XC9000**	**Spartan**	**SpartanXL**	**Virtex**
		√	√			√	√

LDC_1		Transparent Data Latch with Asynchronous Clear and Inverted Gate					
XC3000	**XC4000E**	**XC4000X**	**XC5200**	**XC9000**	**Spartan**	**SpartanXL**	**Virtex**
		√	√			√	√

LDCE		Transparent Data Latch with Asynchronous Clear and Gate Enable					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
		√	√			√	√

LDCE_1		Transparent Data Latch with Asynchronous Clear, Gate Enable, and Inverted Gate					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
		√	√			√	√

LD4CE, LD8CE, LD16CE		Transparent Data Latches with Asynchronous Clear and Gate Enable					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
		√	√			√	√

LDCP		Transparent Data Latch with Asynchronous Clear and Preset					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
							√

LDCP_1		Transparent Data Latch with Asynchronous Clear and Preset and Inverted Gate					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
							√

LDCPE Transparent Data Latch with Asynchronous Clear and Preset and Gate Enable

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
							√

LDCPE_1 Transparent Data Latch with Asynchronous Clear and Preset, Gate Enable, and Inverted Gate

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
							√

LDE Transparent Data Latch with Gate Enable

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
							√

LDE_1 Transparent Data Latch with Gate Enable and Inverted Gate

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
							√

LDP Transparent Data Latch with Asynchronous Preset

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
							√

LDP_1 Transparent Data Latch with Asynchronous Preset and Inverted Gate

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex

							√

LDPE		Transparent Data Latch with Asynchronous Preset and Gate Enable					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
		√				√	√

LDPE_1		Transparent Data Latch with Asynchronous Preset, Gate Enable, and Inverted Gate					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
		√				√	√

Logic Primitives

Combinatorial logic gates that implement the basic Boolean functions are available in all architectures with up to five inputs in all combinations of inverted and non-inverted inputs, and with six to nine inputs non-inverted.

AND2-9		2- to 9-Input AND Gates with Inverted and Non-Inverted Inputs					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√	√	√	√	√

AND12, 16		12- and 16-Input AND Gates with Non-Inverted Inputs					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
			√				√

INV, 4, 8, 16		Single and Multiple Inverters					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**

√	√	√	√	√	√	√	√

MULT_AND Fast Multiplier AND

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
							√

NAND2-9 2- to 9-Input NAND Gates with Inverted and Non-Inverted Inputs

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
√	√	√	√	√	√	√	√

NAND12, 16 12- and 16-Input NAND Gates with Non-Inverted Inputs

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
			√				√

NOR2-9 2- to 9-Input NOR Gates with Inverted and Non-Inverted Inputs

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
√	√	√	√	√	√	√	√

NOR12, 16 12 and 16-Input NOR Gates with Non-Inverted Inputs

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
			√				√

OAND2 2-Input AND Gate with Invertible Inputs

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
		√				√	

ONAND2 2-Input NAND Gate with Invertible Inputs

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
		√				√	

ONOR2 2-Input NOR Gate with Invertible Inputs

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
		√				√	

OOR2 2-Input OR Gate with Invertible Inputs

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
		√				√	

OR2-9 2- to 9-Input OR Gates with Inverted and Non-Inverted Inputs

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	√

OR12, 16 12- and 16-Input OR Gates with Non-Inverted Inputs

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
			√				√

OXNOR2 2-Input Exclusive-NOR Gate with Invertible Inputs

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
		√				√	

OXOR2 2-Input Exclusive-OR Gate with Invertible Inputs

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
		√				√	

SOP3-4 Sum of Products

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	√

WAND1, 4, 8, 16 Open-Drain Buffers

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√					

WOR2AND 2-Input OR Gate with Wired-AND Open-Drain Buffer Output

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√					

XNOR2-9 2- to 9-Input XNOR Gates with Non-Inverted Inputs

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	√

XOR2-9 2- to 9-Input XOR Gates with Non-Inverted Inputs

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
√	√	√	√	√	√	√	√

XORCY XOR for Carry Logic with General Output

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
							√

XORCY_D XOR for Carry Logic with Dual Output

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
							√

XORCY_L XOR for Carry Logic with Local Output

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
							√

Map Elements

Map elements are used in conjunction with logic symbols to constrain the logic to particular CLBs or particular F or H function generators.

CLBMAP Logic-Partitioning Control Symbol

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
√							

F5MAP 5-Input Function Partitioning Control Symbol

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex

			√				

FMAP		F Function Generator Partitioning Control Symbol					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
	√	√	√		√	√	√

HMAP		H Function Generator Partitioning Control Symbol					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
	√	√			√	√	

Memory Elements

The XC4000 and Spartan series architectures have a number of static RAM configurations defined as macros. In the Virtex architecture, they are defined as primitives. These 16- or 32-word RAMs are 1, 2, 4, and 8 bits wide. There are two ROMs in the XC4000 and Spartan series architectures, 16X1 and 32X1.

The Virtex series has dedicated blocks of on-chip 4096-bit single-port and dual-port synchronous RAM. Each port is configured to a specific data width. There are five single-port block RAM primitives and 30 dual-port block RAM primitives.

RAM16X1		16-Deep by 1-Wide Static RAM					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
	√	√					

RAM16X1D		16-Deep by 1-Wide Static Dual Port Synchronous RAM					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
	√	√			√	√	√

RAM16X1D_1	16-Deep by 1-Wide Static Dual Port Synchronous RAM with Negative-Edge Clock

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
							√

RAM16X1S 16-Deep by 1-Wide Static Synchronous RAM

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√			√	√	√

RAM16X1S_1 16-Deep by 1-Wide Static Synchronous RAM with Negative-Edge Clock

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
							√

RAM16X2 16-Deep by 2-Wide Static RAM

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√					

RAM16X2D 16-Deep by 2-Wide Static Dual Port Synchronous RAM

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√			√	√	√

RAM16X2S 16-Deep by 2-Wide Static Synchronous RAM

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√			√	√	√

RAM16X4 16-Deep by 4-Wide Static RAM

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√					

RAM16X4D 16-Deep by 4-Wide Static Dual Port Synchronous RAM

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√			√	√	√

RAM16X4S 16-Deep by 4-Wide Static Synchronous RAM

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√			√	√	√

RAM16X8 16-Deep by 8-Wide Static RAM

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√					

RAM16X8D 16-Deep by 8-Wide Static Dual Port Synchronous RAM

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√			√	√	√

RAM16X8S 16-Deep by 8-Wide Static Synchronous RAM

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
	√	√			√	√	√

RAM32X1 32-Deep by 1-Wide Static RAM

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
	√	√					

RAM32X1S 32-Deep by 1-Wide Static Synchronous RAM

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
	√	√			√	√	√

RAM32X1S_1 32-Deep by 1-Wide Static Synchronous RAM with Negative-Edge Clock

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
							√

RAM32X2 32-Deep by 2-Wide Static RAM

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
	√	√					

RAM32X2S 32-Deep by 2-Wide Static Synchronous RAM

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
	√	√			√	√	√

RAM32X4 32-Deep by 4-Wide Static RAM

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	SpartanXL	Virtex
	√	√					

RAM32X4S		32-Deep by 4-Wide Static Synchronous RAM					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
	√	√			√	√	√

RAM32X8		32-Deep by 8-Wide Static RAM					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
	√	√					

RAM32X8S		32-Deep by 8-Wide Static Synchronous RAM					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
	√	√			√	√	√

RAMB4_Sn		4096-Bit Single-Port Synchronous Block RAM with Port Width (n) Configured to 1, 2, 4, 8, or 16 Bits (5 primitives)					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
							√

RAMB4_Sn_Sn		4096-Bit Dual-Port Synchronous Block RAM with Port Width (n) Configured to 1, 2, 4, 8, or 16 Bits (30 primitives)					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
							√

ROM16X1		16-Deep by 1-Wide ROM					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**

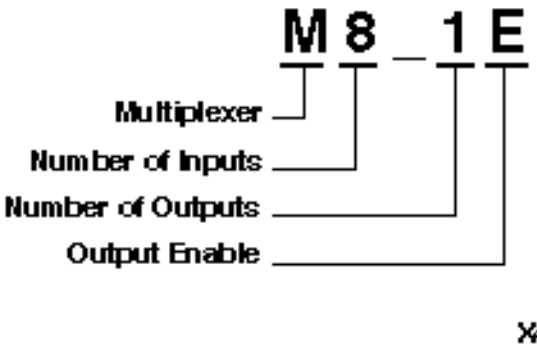
	√	√			√	√	

ROM32X1		32-Deep by 1-Wide ROM					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
	√	√			√	√	

Multiplexers

The multiplexer naming convention shown in the following figure indicates the number of inputs and outputs and if an enable is available. There are a number of TTL 7400-type multiplexers that have active-Low or inverted outputs.

Figure 2-7Multiplexer Naming Convention



CY_MUX		2-to-1 Multiplexer for Carry Logic					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
			√				

F5_MUX		2-to-1 Lookup Table Multiplexer					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
			√				

M2_1 2-to-1 Multiplexer

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	√

M2_1B1 2-to-1 Multiplexer with D0 Inverted

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	√

M2_1B2 2-to-1 Multiplexer with D0 and D1 Inverted

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	√

M2_1E 2-to-1 Multiplexer with Enable

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	√

M4_1E 4-to-1 Multiplexer with Enable

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	√

M8_1E 8-to-1 Multiplexer with Enable

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	√

M16_1E 16-to-1 Multiplexer with Enable

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	√

MUXCY 2-to-1 Multiplexer for Carry Logic with General Output

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	Spartan XL	Virtex
							√

MUXCY_D 2-to-1 Multiplexer for Carry Logic with Dual Output

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	Spartan XL	Virtex
							√

MUXCY_L 2-to-1 Multiplexer for Carry Logic with Local Output

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	Spartan XL	Virtex
							√

MUXF5 2-to-1 Lookup Table Multiplexer with General Output

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	Spartan XL	Virtex
							√

MUXF5_D 2-to-1 Lookup Table Multiplexer with Dual Output

XC3000	XC4000E	XC4000X	XC5200	XC9000	Spartan	Spartan XL	Virtex
							√

MUXF5_L		2-to-1 Lookup Table Multiplexer with Local Output					
XC3000	**XC4000E**	**XC4000X**	**XC5200**	**XC9000**	**Spartan**	**SpartanXL**	**Virtex**
							√

MUXF6		2-to-1 Lookup Table Multiplexer with General Output					
XC3000	**XC4000E**	**XC4000X**	**XC5200**	**XC9000**	**Spartan**	**SpartanXL**	**Virtex**
							√

MUXF6_D		2-to-1 Lookup Table Multiplexer with Dual Output					
XC3000	**XC4000E**	**XC4000X**	**XC5200**	**XC9000**	**Spartan**	**SpartanXL**	**Virtex**
							√

MUXF6_L		2-to-1 Lookup Table Multiplexer with Local Output					
XC3000	**XC4000E**	**XC4000X**	**XC5200**	**XC9000**	**Spartan**	**SpartanXL**	**Virtex**
							√

OMUX2		2-to-1 Multiplexer					
XC3000	**XC4000E**	**XC4000X**	**XC5200**	**XC9000**	**Spartan**	**SpartanXL**	**Virtex**
		√				√	

X74_150		16-to-1 Multiplexer with Active-Low Enable and Output					
XC3000	**XC4000E**	**XC4000X**	**XC5200**	**XC9000**	**Spartan**	**SpartanXL**	**Virtex**
√	√	√	√	√	√	√	

X74_151		8-to-1 Multiplexer with Active-Low Enable and Complementary Outputs					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√	√	√	√	

X74_152		8-to-1 Multiplexer with Active-Low Output					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√	√	√	√	

X74_153		Dual 4-to-1 Multiplexer with Active-Low Enables and Common Select Input					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√	√	√	√	

X74_157		Quadruple 2-to-1 Multiplexer with Common Select and Active-Low Enable					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√	√	√	√	

X74_158		Quadruple 2-to-1 Multiplexer with Common Select, Active-Low Enable, and Active-Low Outputs					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√	√	√	√	

X74_298		Quadruple 2-Input Multiplexer with Storage and Negative-Edge Clock					

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	

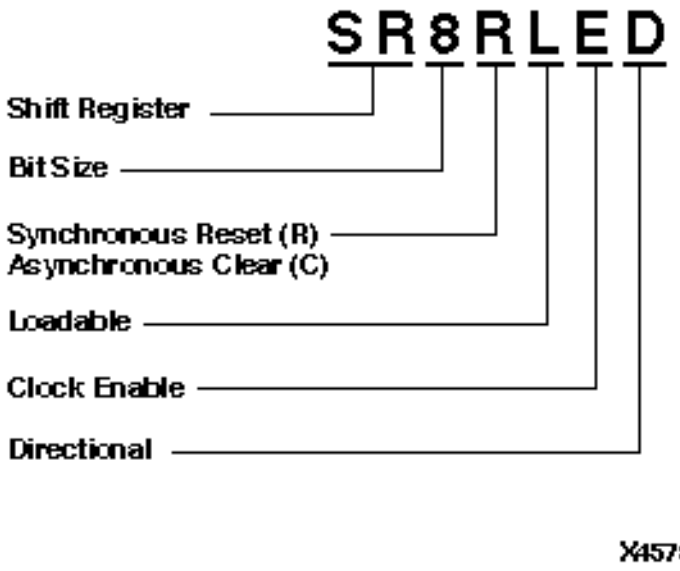
X74_352	Dual 4-to-1 Multiplexer with Active-Low Enables and Outputs

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	

Shift Registers

Shift registers are available in a variety of sizes and capabilities. The naming convention shown in the following figure illustrates available features.

Figure 2-8Shift Register Naming Convention



SR4CE, SR8CE, SR16CE	4-, 8-, 16-Bit Serial-In Parallel-Out Shift Registers with Clock Enable and Asynchronous Clear

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	√

SR4CLE, SR8CLE, SR16CLE	4-, 8-, 16-Bit Loadable Serial/Parallel-In Parallel-Out Shift Registers with Clock Enable and Asynchronous Clear						
XC3000	**XC4000E**	**XC4000X**	**XC5200**	**XC9000**	**Spartan**	**SpartanXL**	**Virtex**
√	√	√	√	√	√	√	√

SR4CLED, SR8CLED, SR16CLED	4-, 8-, 16-Bit Shift Registers with Clock Enable and Asynchronous Clear						
XC3000	**XC4000E**	**XC4000X**	**XC5200**	**XC9000**	**Spartan**	**SpartanXL**	**Virtex**
√	√	√	√	√	√	√	√

SR4RE, SR8RE, SR16RE	4-, 8-, 16-Bit Serial-In Parallel-Out Shift Registers with Clock Enable and Synchronous Reset						
XC3000	**XC4000E**	**XC4000X**	**XC5200**	**XC9000**	**Spartan**	**SpartanXL**	**Virtex**
√	√	√	√	√	√	√	√

SR4RLE, SR8RLE, SR16RLE	4-, 8-, 16-Bit Loadable Serial/Parallel-In Parallel-Out Shift Registers with Clock Enable and Synchronous Reset						
XC3000	**XC4000E**	**XC4000X**	**XC5200**	**XC9000**	**Spartan**	**SpartanXL**	**Virtex**
√	√	√	√	√	√	√	√

SR4RLED, SR8RLED, SR16RLED	4-, 8-, 16-Bit Shift Registers with Clock Enable and Synchronous Reset						
XC3000	**XC4000E**	**XC4000X**	**XC5200**	**XC9000**	**Spartan**	**SpartanXL**	**Virtex**
√	√	√	√	√	√	√	√

SRL16		16-Bit Shift Register Look-Up-Table (LUT)					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
							√

SRL16_1		16-Bit Shift Register Look-Up-Table (LUT) with Negative-Clock Edge					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
							√

SRL16E		16-Bit Shift Register Look-Up-Table (LUT) with Clock Enable					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
							√

SRL16E_1		16-Bit Shift Register Look-Up-Table (LUT) with Negative-Edge Clock and Clock Enable					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
							√

X74_164		8-Bit Serial-In Parallel-Out Shift Register with Active-Low Asynchronous Clear					
XC3000	**XC4000 E**	**XC4000 X**	**XC5200**	**XC9000**	**Spartan**	**Spartan XL**	**Virtex**
√	√	√	√	√	√	√	

X74_165S	8-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	

X74_194	4-Bit Loadable Bidirectional Serial/Parallel-In Parallel-Out Shift Register

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	

X74_195	4-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	

Shifters

Shifters are barrel shifters (BRLSHFT) of four and eight bits.

BRLSHFT4, 8	4-, 8-Bit Barrel Shifters

XC3000	XC4000 E	XC4000 X	XC5200	XC9000	Spartan	Spartan XL	Virtex
√	√	√	√	√	√	√	√